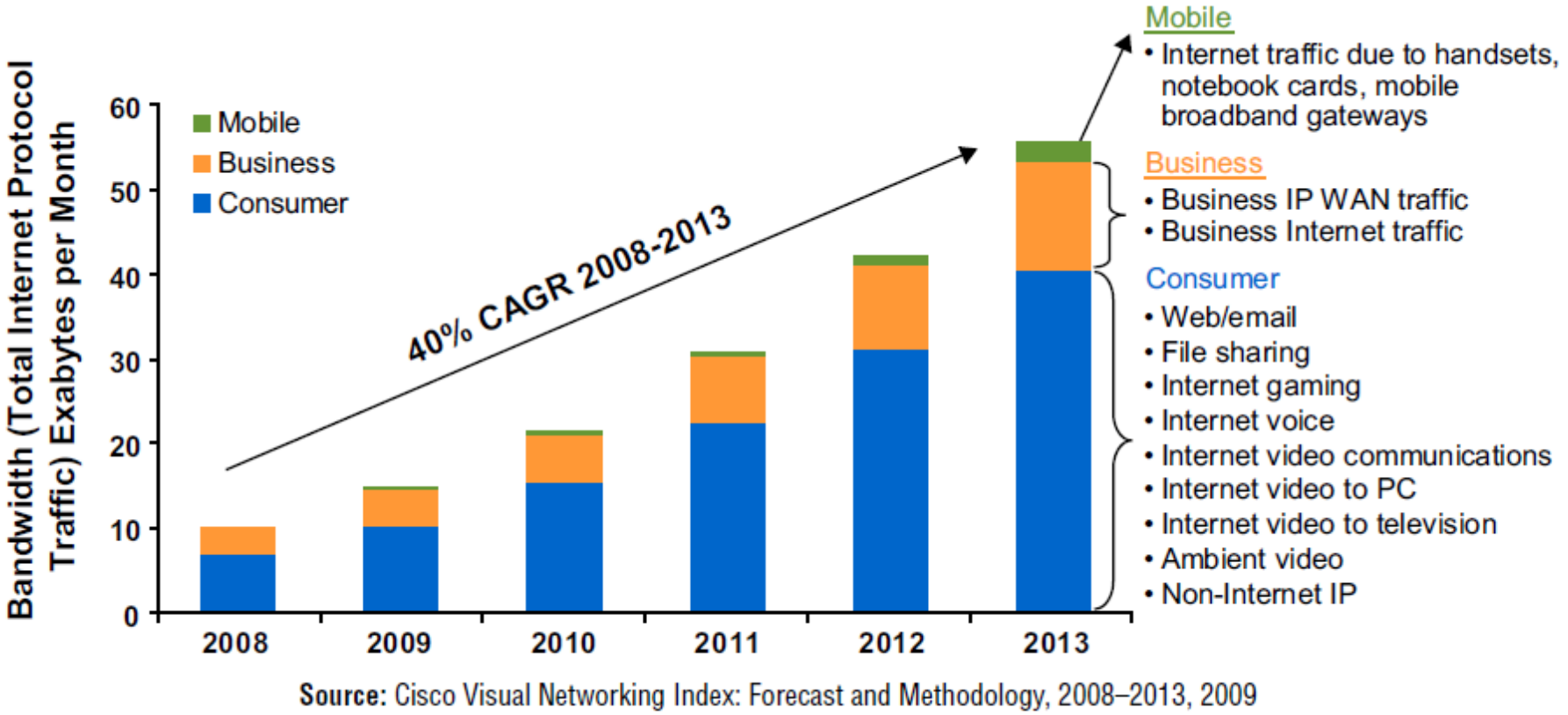
Familias Lógicas

Introducción a los Sistemas Lógicos y Digitales

2017

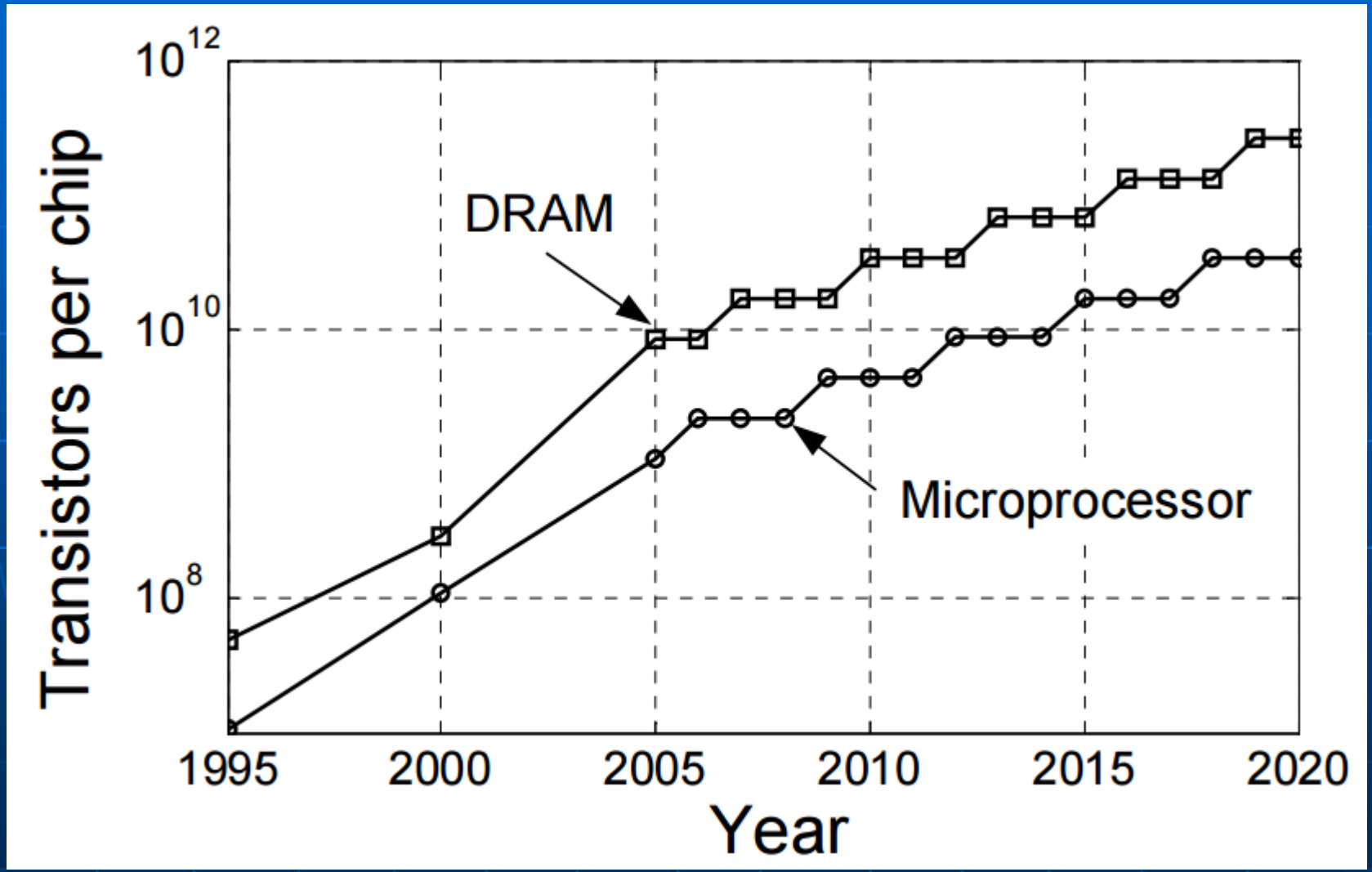
Crecimiento del tráfico global del protocolo de internet



Source: Cisco Visual Networking Index: Forecast and Methodology, 2008–2013, 2009

Necesidad de tecnologías más rápidas, de menor consumo y mayor densidad de integración

Evolución de la densidad de integración



Familias Lógicas

Las Familias Lógicas son tecnologías que permiten implementar las funciones tanto lógicas como matemáticas en el sistema binario.

CLASIFICACIÓN:
Dependiendo de la tecnología empleada:

BIPOLAR	Lógica TTL (Transistor-Transistor Logic). Lógica ECL (Emitter-Coupled Logic). CML (Current Mode Logic)
MOS	Lógica CMOS (Complemmentary Metal-Oxide Semiconductor). LVDS (Low Voltage Differential Signaling)
BIPOLAR-MOS	Lógica BiCMOS.
OTRAS	Lógica GaAs (Galio-Arsénico), etc.. Lógica eléctrica (relays, llaves, etc.). Lógica neumática. Lógica óptica….ETC…

NOTA: Aquí se tratarán los primeros 3 grupos.

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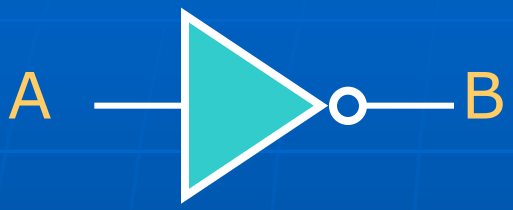
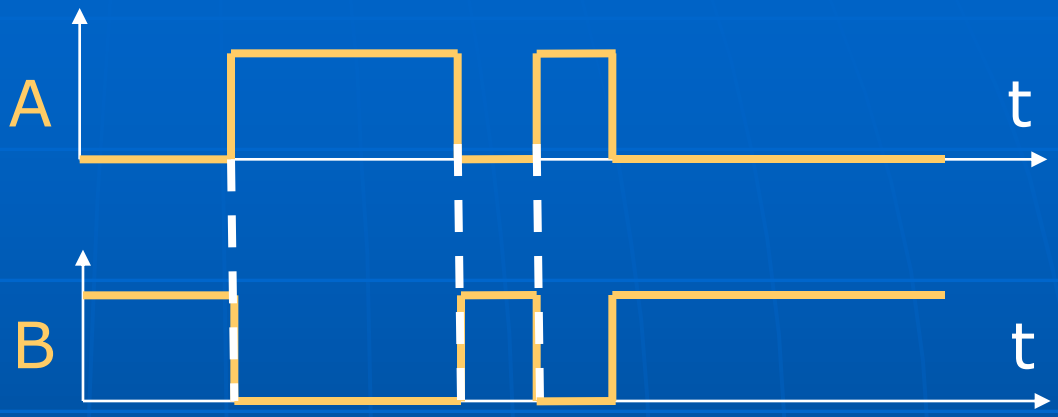
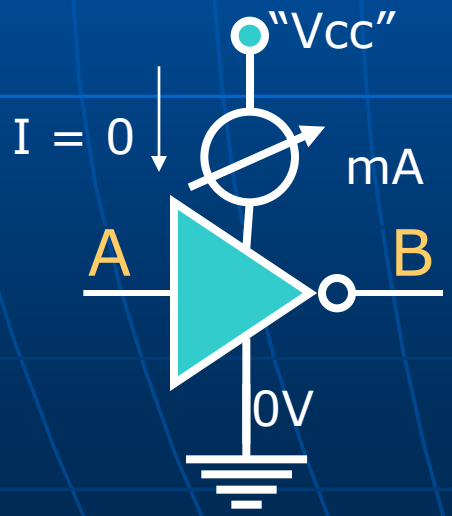
Velocidad de respuesta infinita (retardos nulos)





Consumo de energía nulo



Esto requiere que el dispositivo no consuma corriente de la fuente de alimentación. Además impone otra condición y es que si hay una carga conectada a la salida del mismo la misma debe ser infinita para no "pedirle" corriente al circuito.

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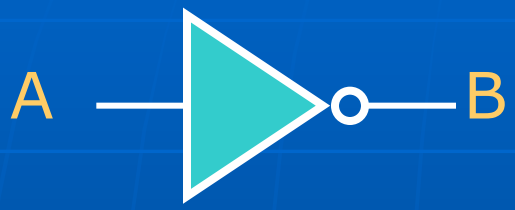
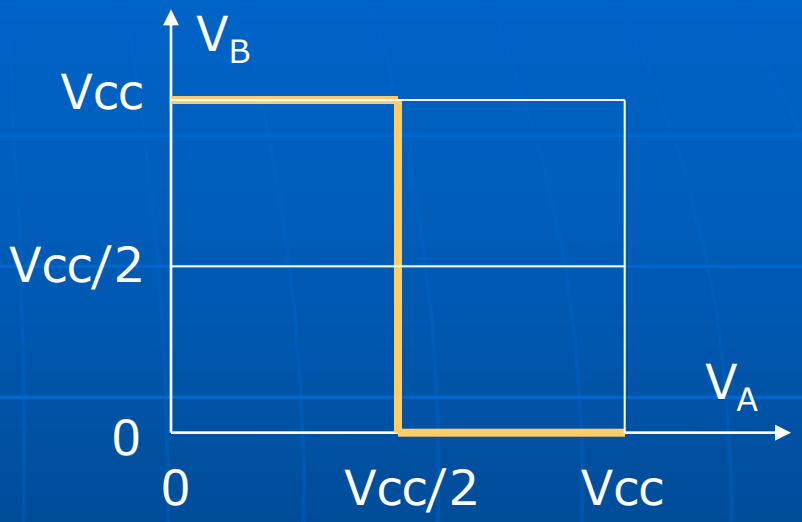
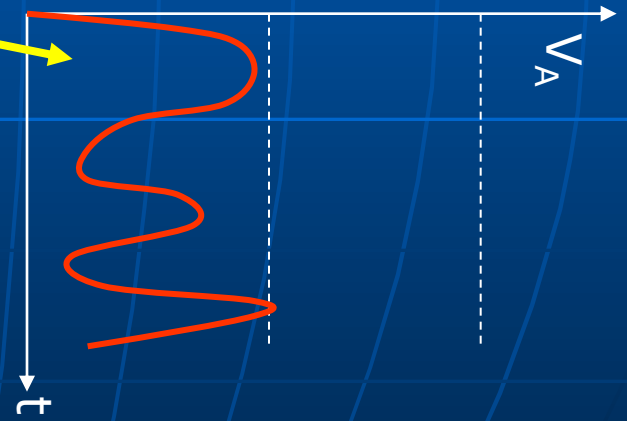
Inmunidad al ruido del 50% de la tensión de alimentación





Mientras la señal de entrada no supere los Vcc/2 Volts el inversor sigue reconociendo el "0" a su entrada.

Lo mismo sucede para el "1". De esta manera se tiene un "Márgen de ruido" de Vcc/2 ó 50% para cada nivel lógico. Es el márgen máximo que se puede obtener.



NOTA: Aquí no se considera el concepto de Schmitt Trigger que se planteará luego.

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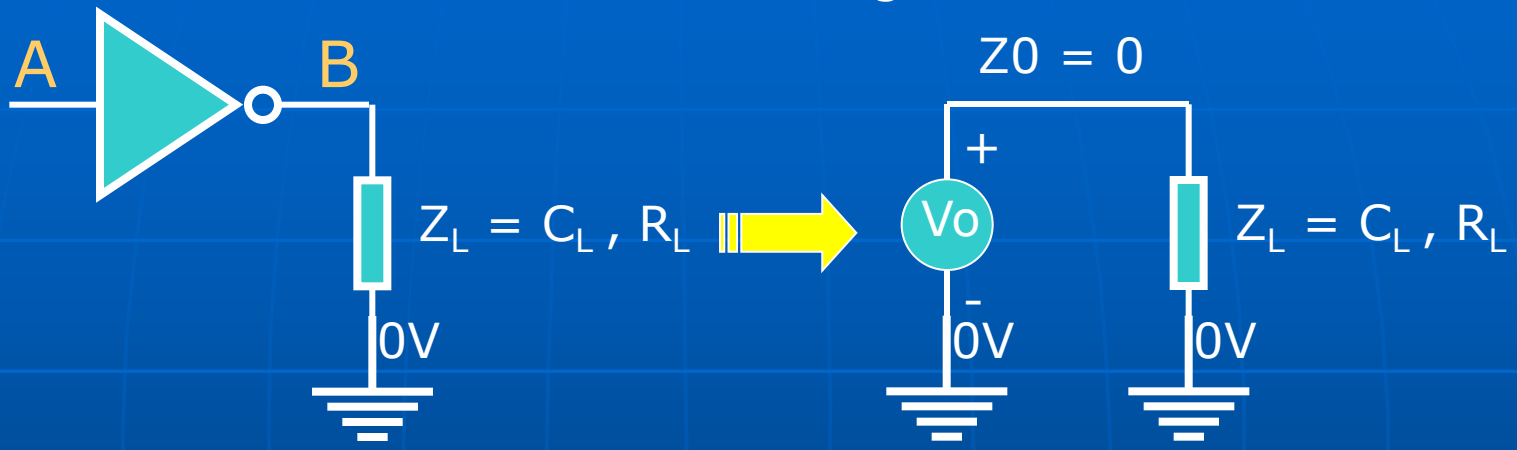
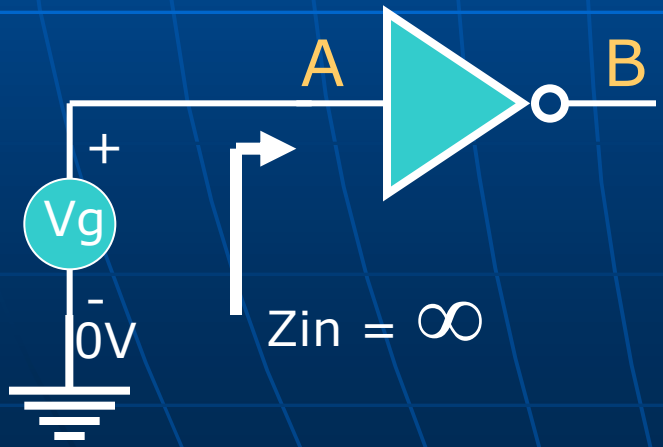
Capacidad de carga infinita:

La tensión de salida no varía con la carga.



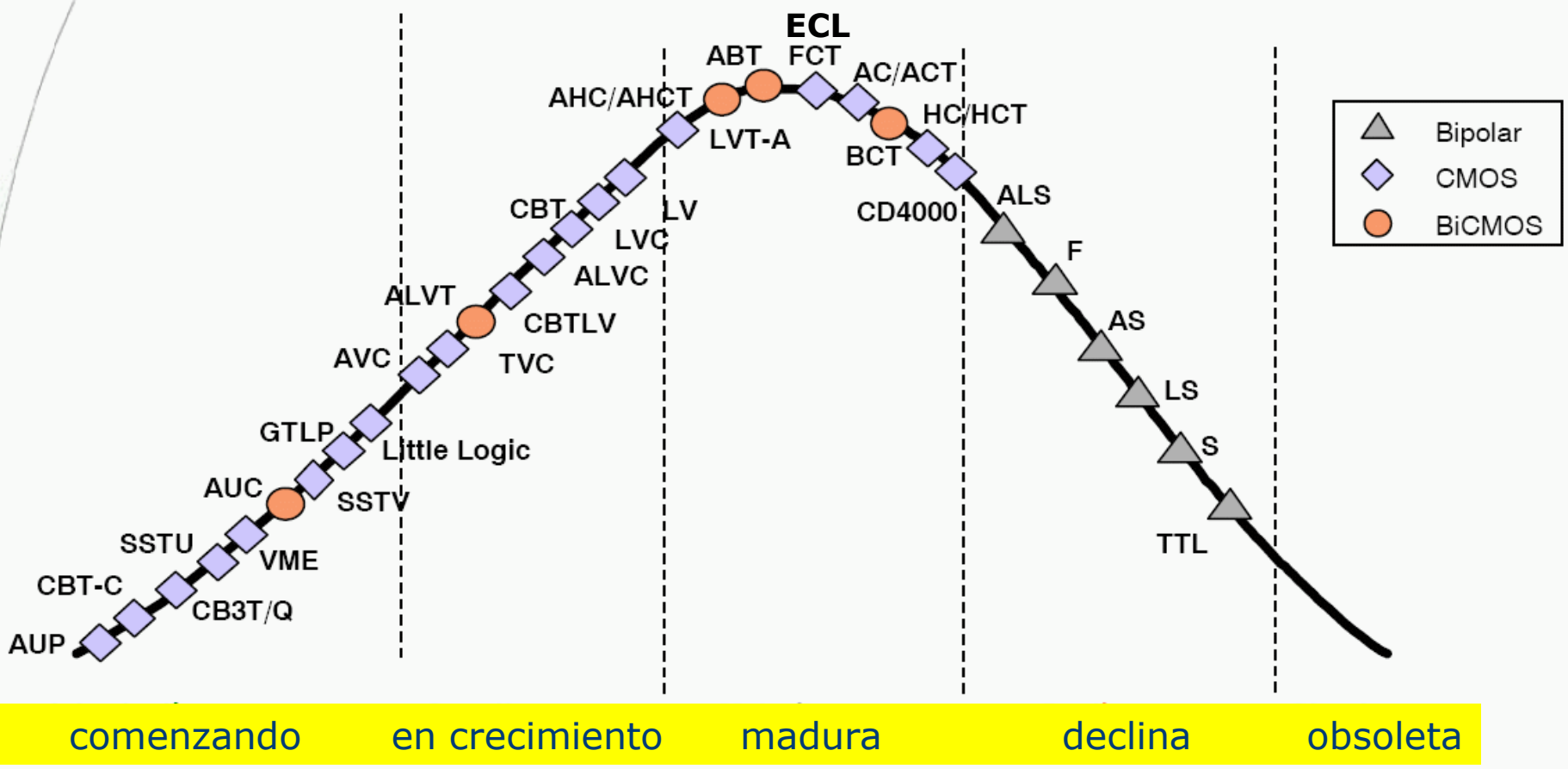
Impedancia de entrada infinita:

La impedancia de entrada al ser infinita no consume corriente de la fuente a la cual esté conectada.



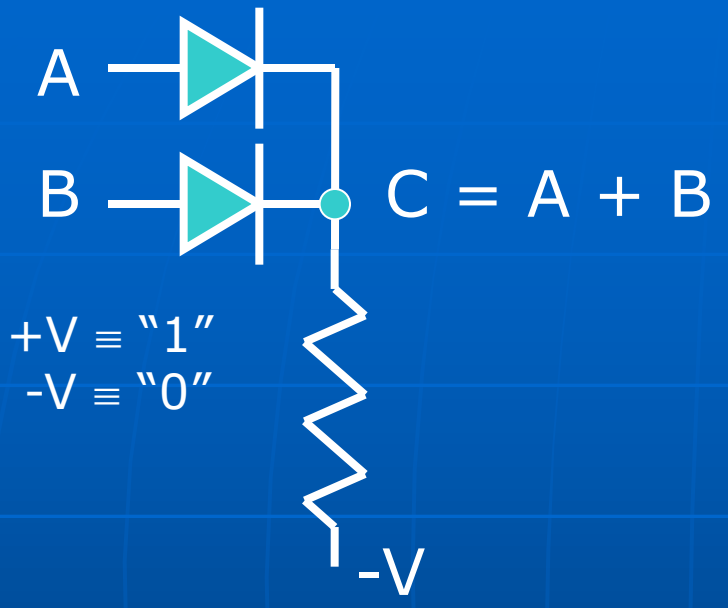
Familias Lógicas

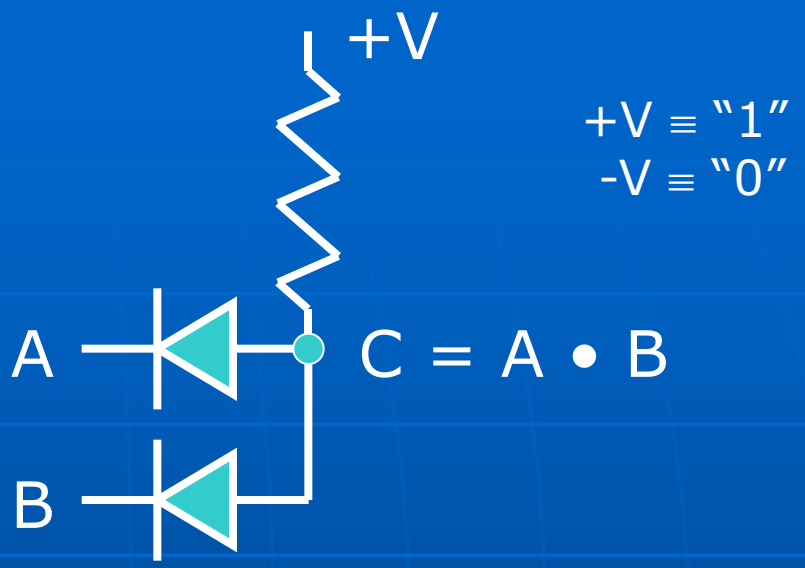
EVOLUCIÓN DE LAS TECNOLOGÍAS DE SEMICONDUCTORES DIGITALES

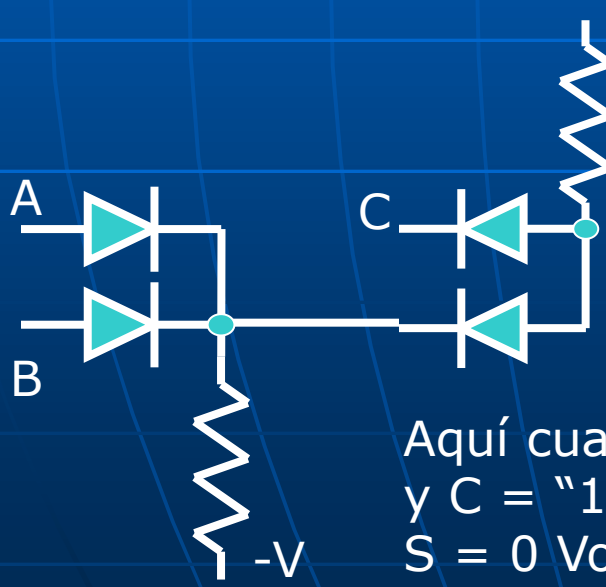


Familias Lógicas

LÓGICA DIODO (DL)







Aquí cuando A = B = "0"
y C = "1" ➔ La tensión en
S = 0 Volts si las R son iguales.

Esta lógica no permite cascadas de compuertas ni puede resolver negaciones.
Necesita fuente partida (+V y –V)

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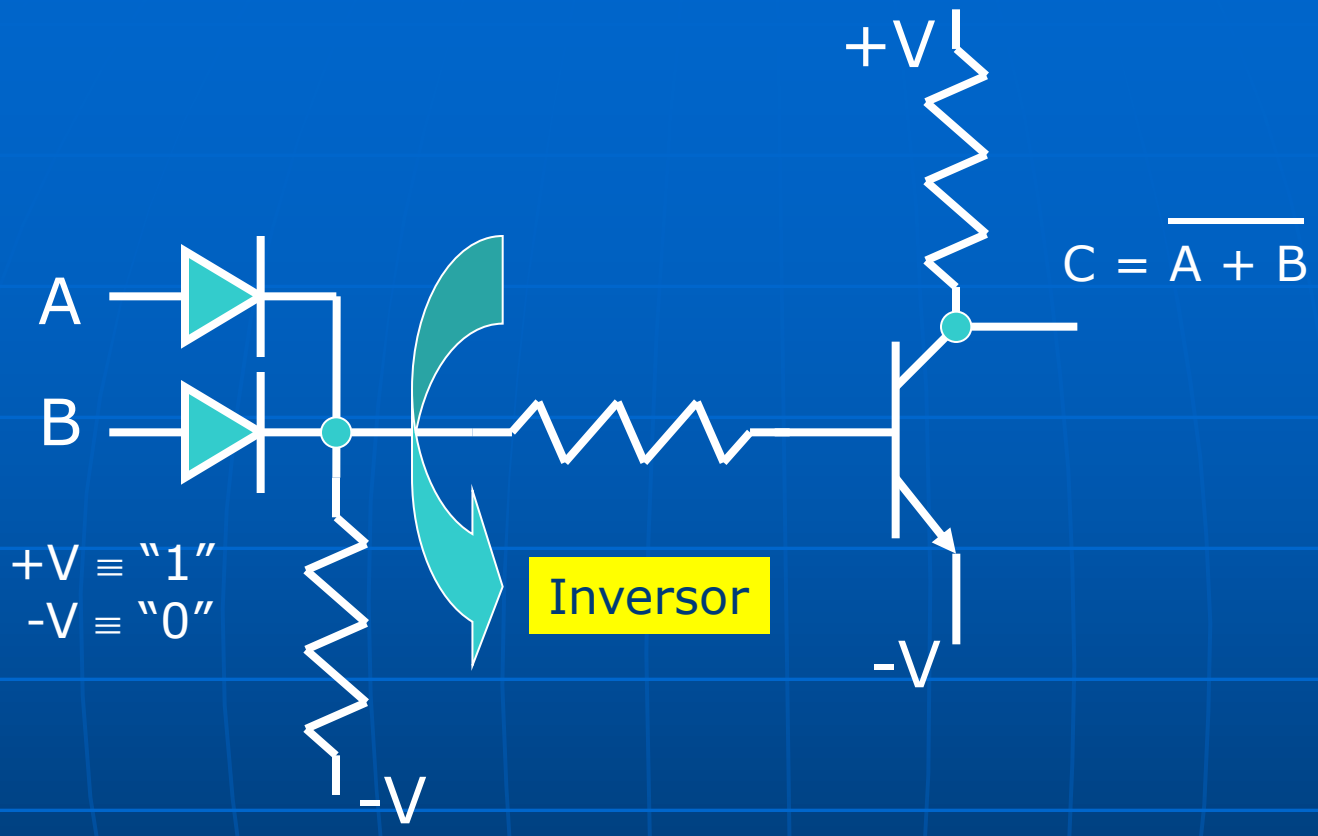
LÓGICA DIODO-TRANSISTOR (DTL)



Esta lógica permite realizar negaciones ➔ implementa cualquier función.
Como hay ganancia de tensión permite cascada de compuertas.
Problemas serios por tener un márgen de ruido pequeño y retardos elevados. Además requiere fuente partida.

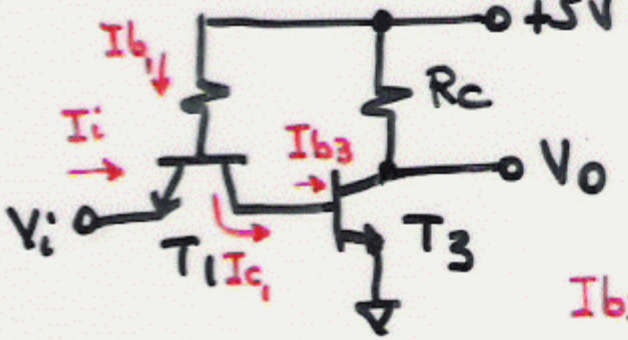
PRÓXIMO PASO ➔ LÓGICA TRANSISTOR-TRANSISTOR (TTL)

Lógica TTL

Evolución

serie 74, serie 74L, serie 74S (Schottky),
serie 74LS (Schottky de bajo consumo),
serie 74ALS, 74F,
versiones de baja tensión de alimentación.

INVERSOR



$I_{b3} = I_{b1} + I_{c1}$

1) $V_i = H$

T_1 modo inverso

E→C, C→E

$I_i = \alpha_i I_{b3} \rightarrow I_{b1} \simeq I_{b3}$

└ muy bajo (0.02) para sat. a T_3 con I_i chica.

$V_{CE\,SAT} \simeq 0.2V.$

2) $V_i = L \rightarrow V_{BE_1}$ directa $\sim 0.75V$

$\rightarrow V_{CE_1}$ SATURADO $\rightarrow T_3$ OFF

Desventaja: Rc alta → gran retardo.

Rc baja → gran consumo.

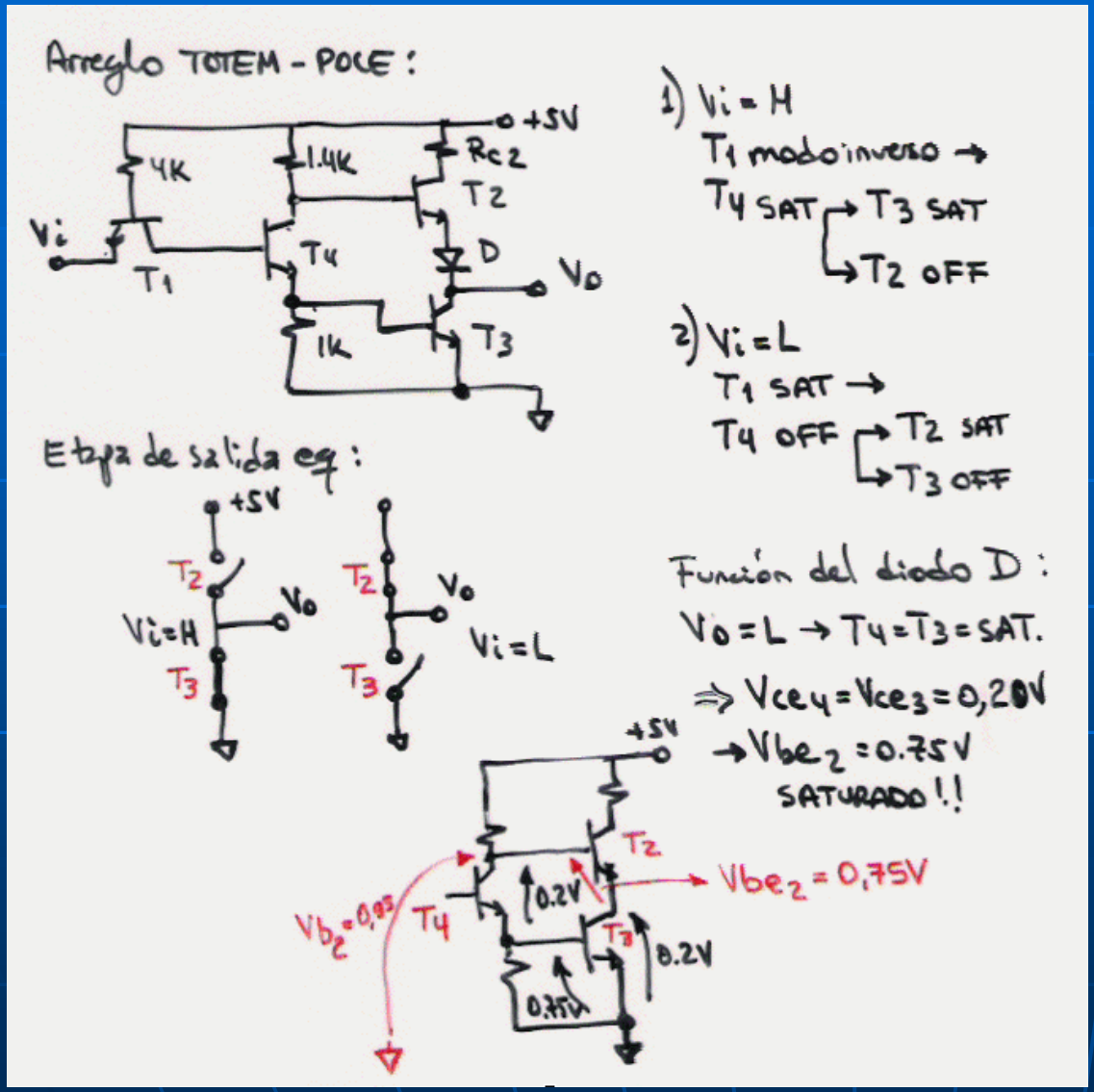
Este tipo de configuración permite:

>Trabajar con fuente simple (+5V).

>Consumir poca corriente a la entrada (alta impedancia de entrada).

>Problemas con retardos ya que Rc debe ser pequeña y eso implica gran consumo.

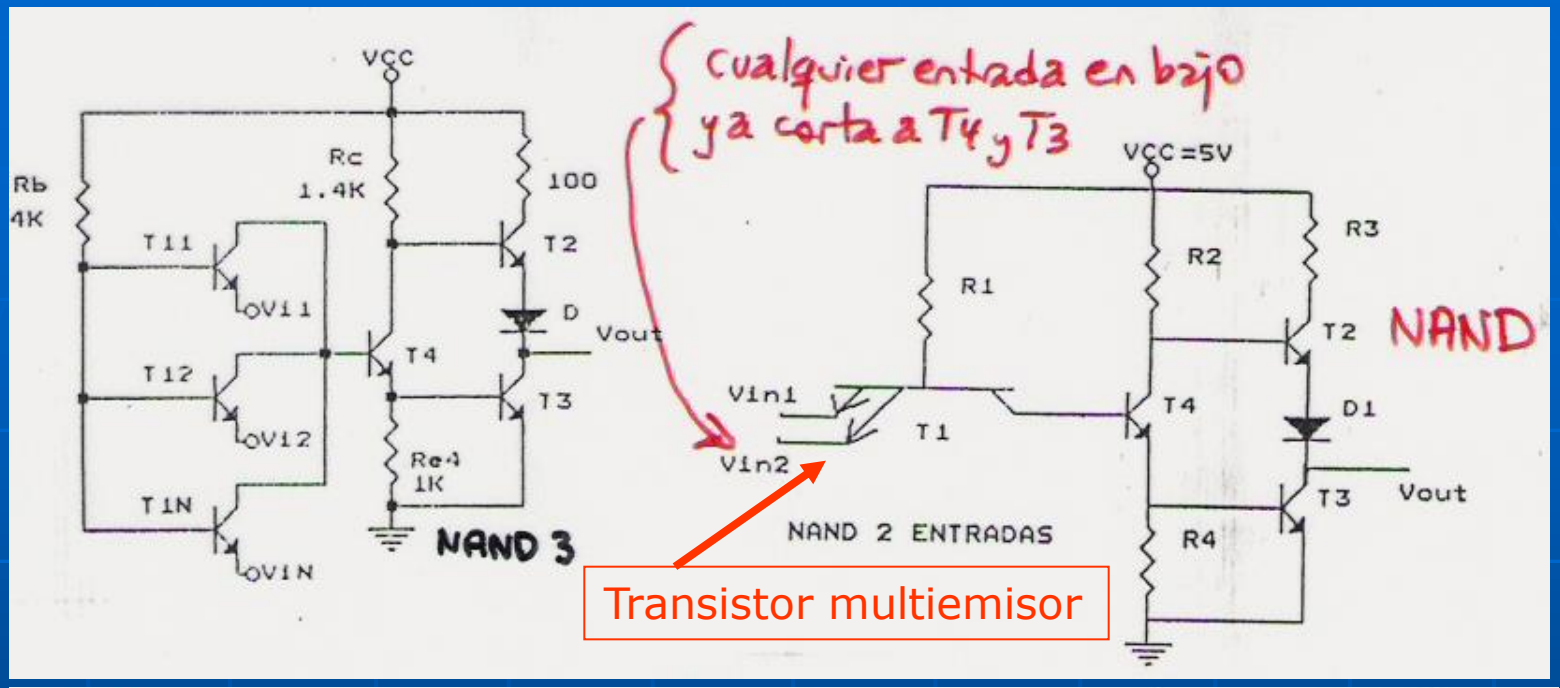
Familias Lógicas

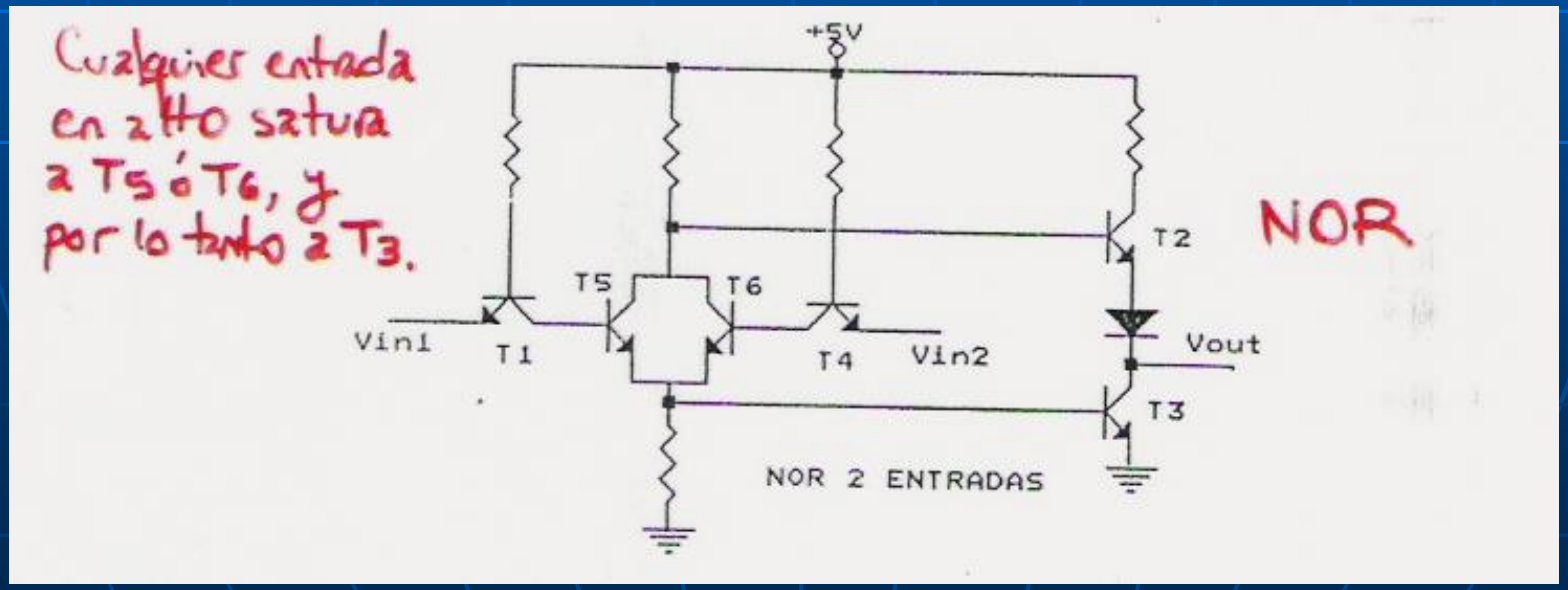


El diodo evita que se sature T2 junto con T3 (T2 debe estar cortado cuando en ViH. Con la inclusión de D, se necesitarían 0,6V adicionales para hacer conducir a T2.

Familias Lógicas

FAMILIA TTL

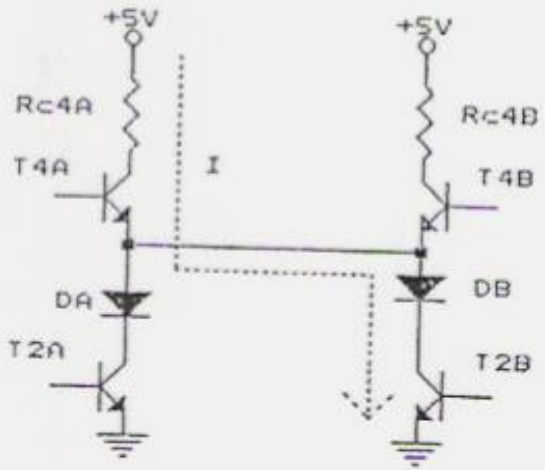




Familias Lógicas

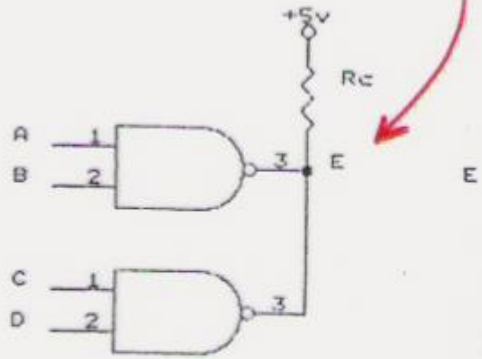
Porqué se necesitan salidas OPEN COLLECTOR

???

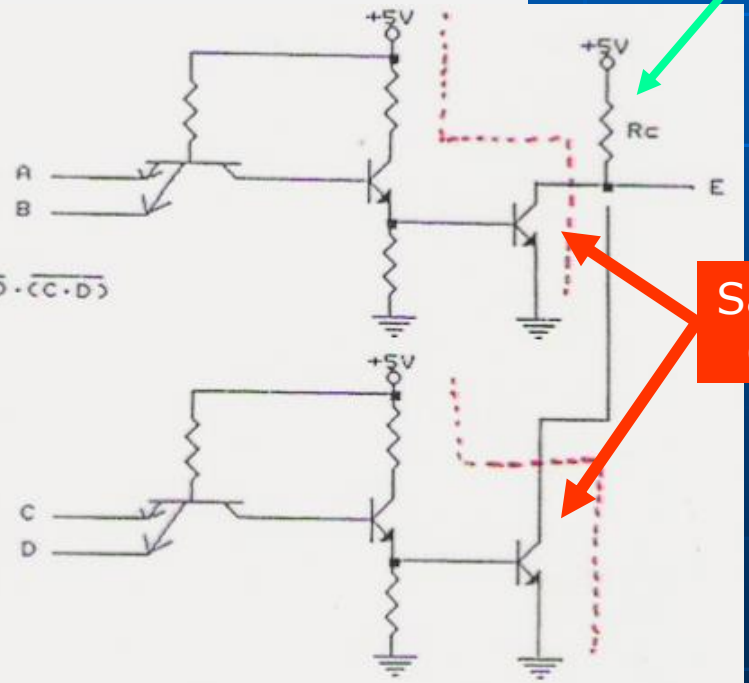


Si se unen salidas TTL y por ejemplo la salida de la compuerta A está en H y la de B en L, circularía una I muy grande que puede dañar a los transistores.

Función AND



$E = \overline{(A \cdot B)} \cdot \overline{(C \cdot D)}$

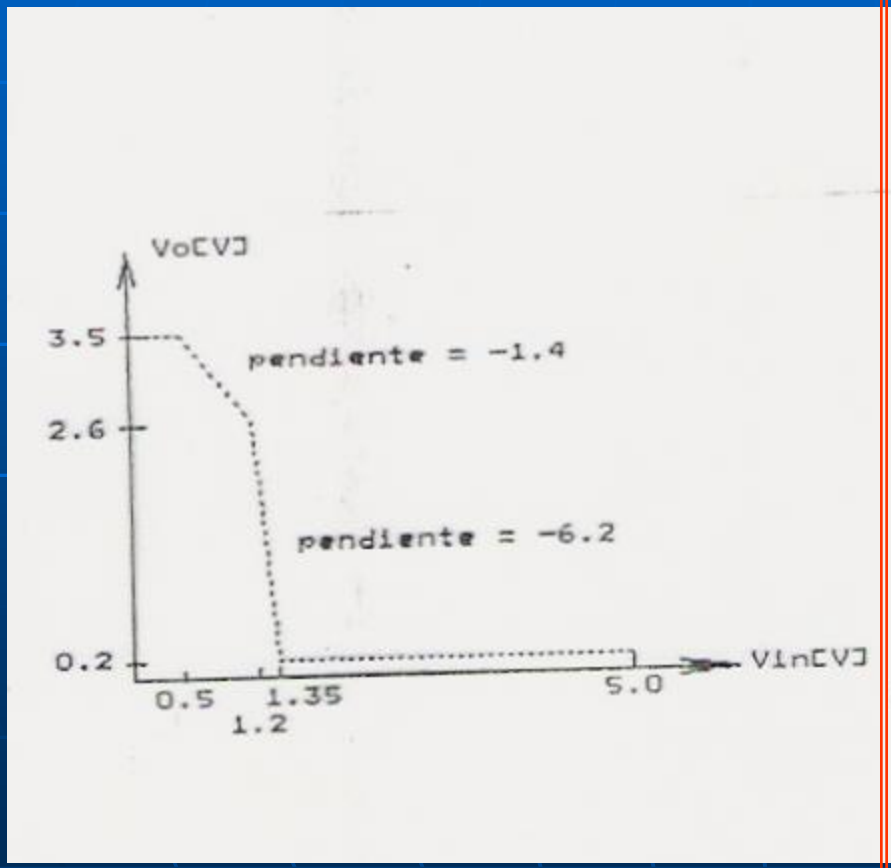


R externa

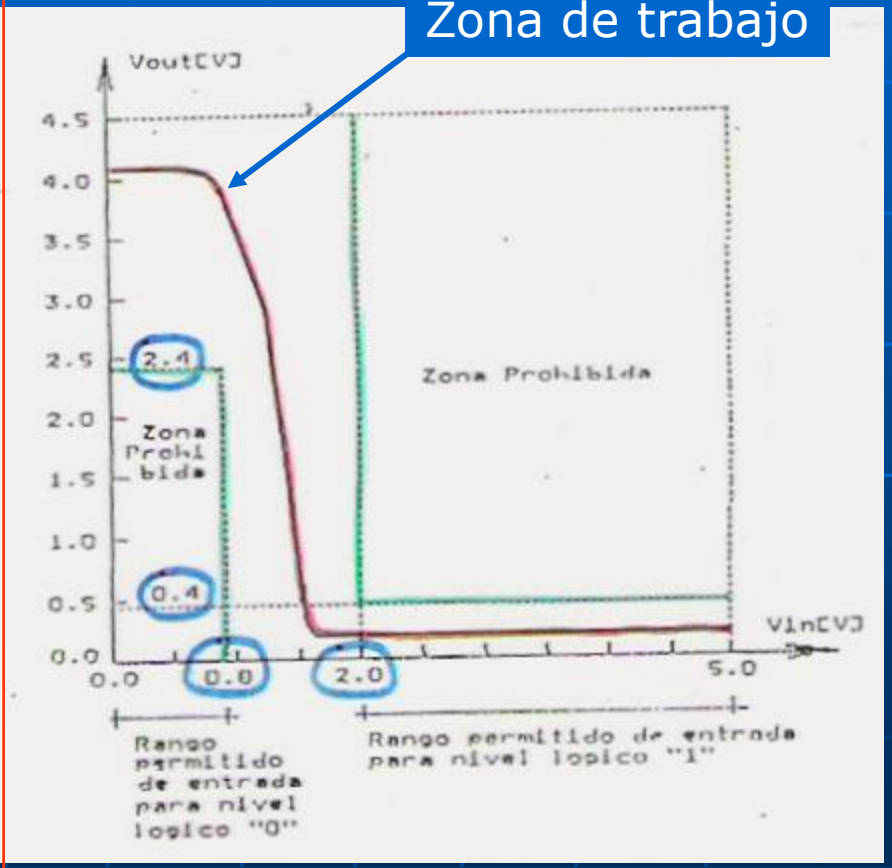
Salidas con transistores con colector abierto

Familias Lógicas

Función de transferencia idealizada de un inversor TTL



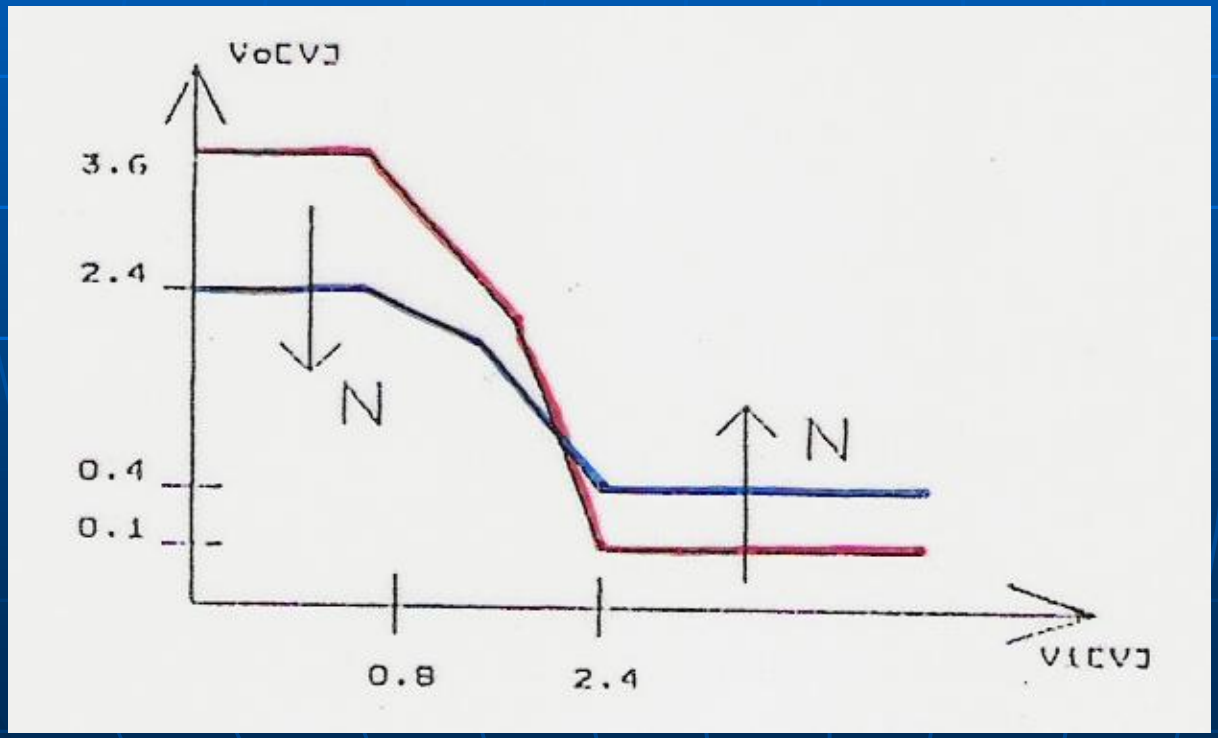
Función de transferencia típica de un inversor con rangos de funcionamiento garantizados por el fabricante



Familias Lógicas

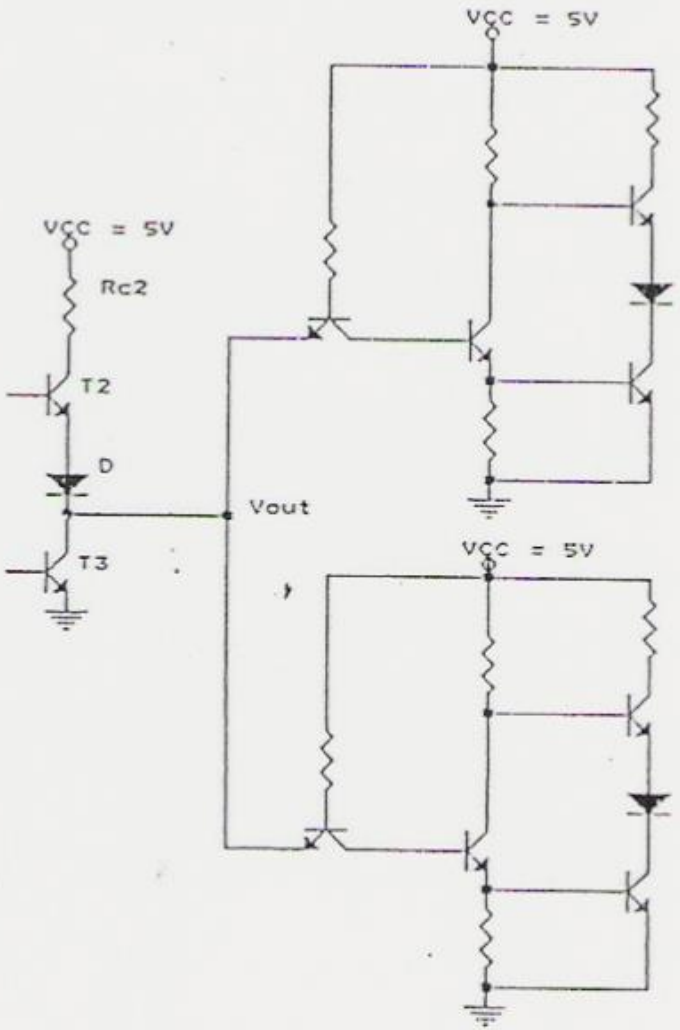
Efecto de incrementar la carga a una compuerta

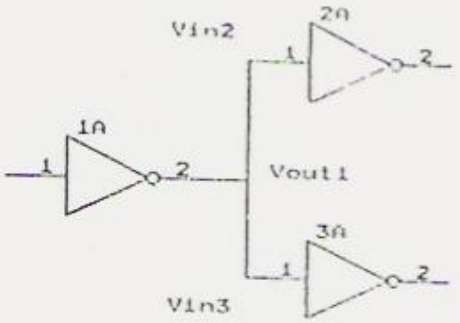
La tensión en nivel L de la salida irá creciendo a medida que aumenta la corriente de carga. Lo contrario pasa en el nivel H.
El resultado es una degradación del márgen de ruido.



Familias Lógicas

FAMILIA TTL





$$\frac{IoHmáx}{IoHnorm} = \frac{400uA}{40uA} = 10U.L$$

$$\frac{IoLmáx}{IoLnorm} = \frac{8.0mA}{1.6mA} = 5U.L$$

$$\frac{IiHmáx}{IiHnorm} = \frac{20uA}{40uA} = 0.5U.L$$

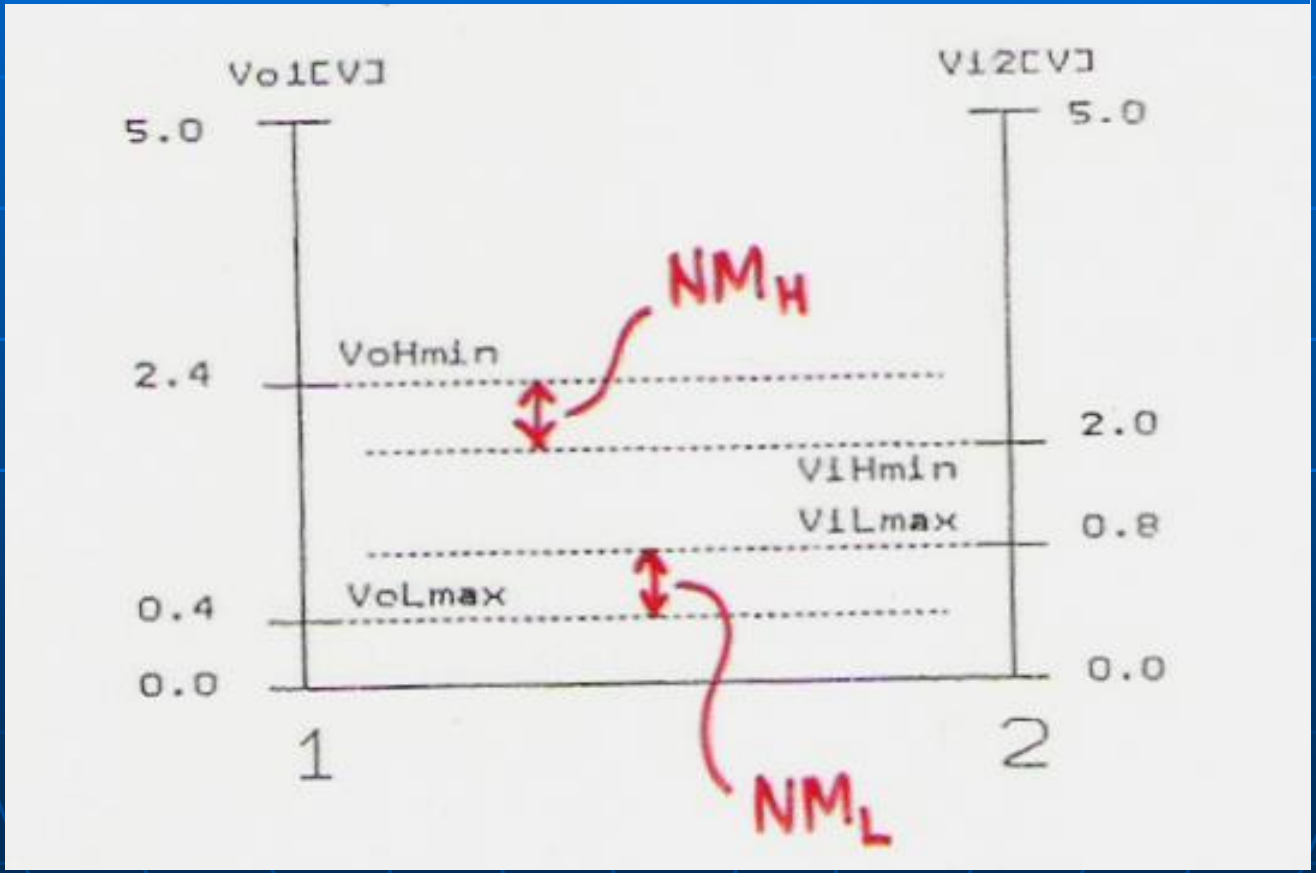
$$\frac{IiLmáx}{IiLnorm} = \frac{0.4mA}{1.6mA} = 0.25U.L$$

$$\begin{cases} 1\,UL_H = 40\mu A \\ 1\,UL_L = 1{,}6mA \end{cases}$$

Familias Lógicas

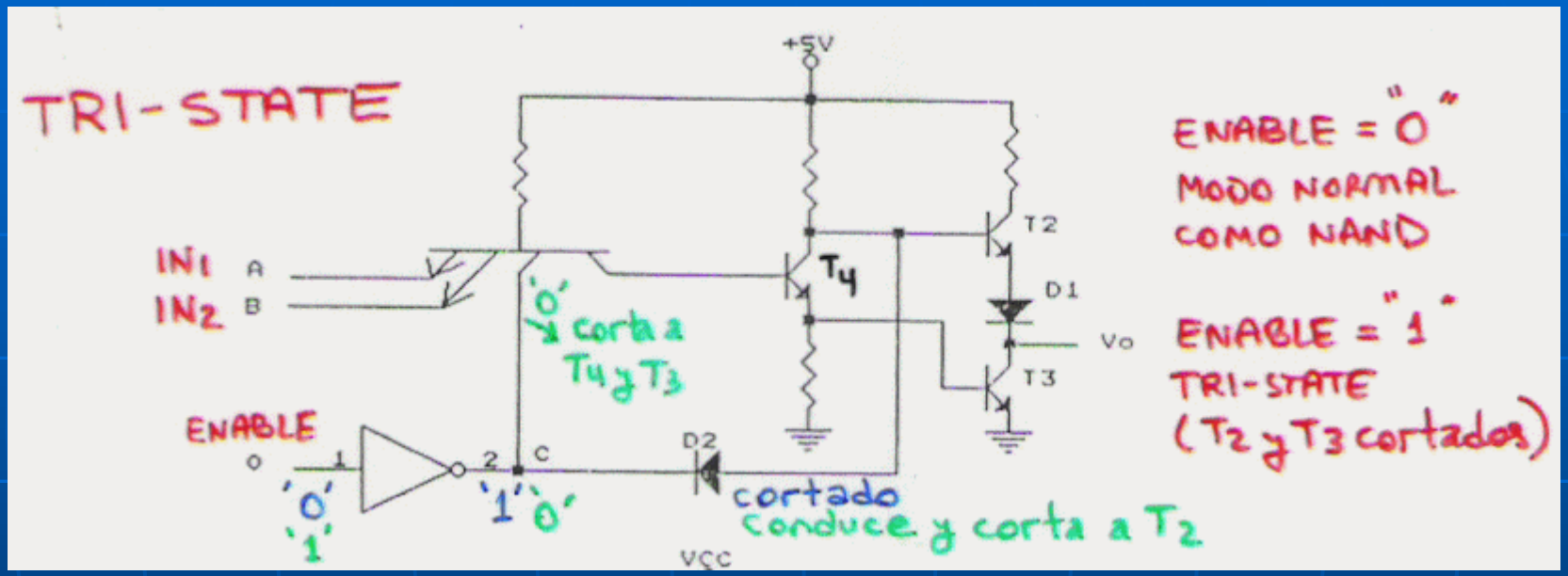
Márgen de ruido en nivel alto y bajo

Salida de compuerta 1 Entrada de compuerta 2



Familias Lógicas

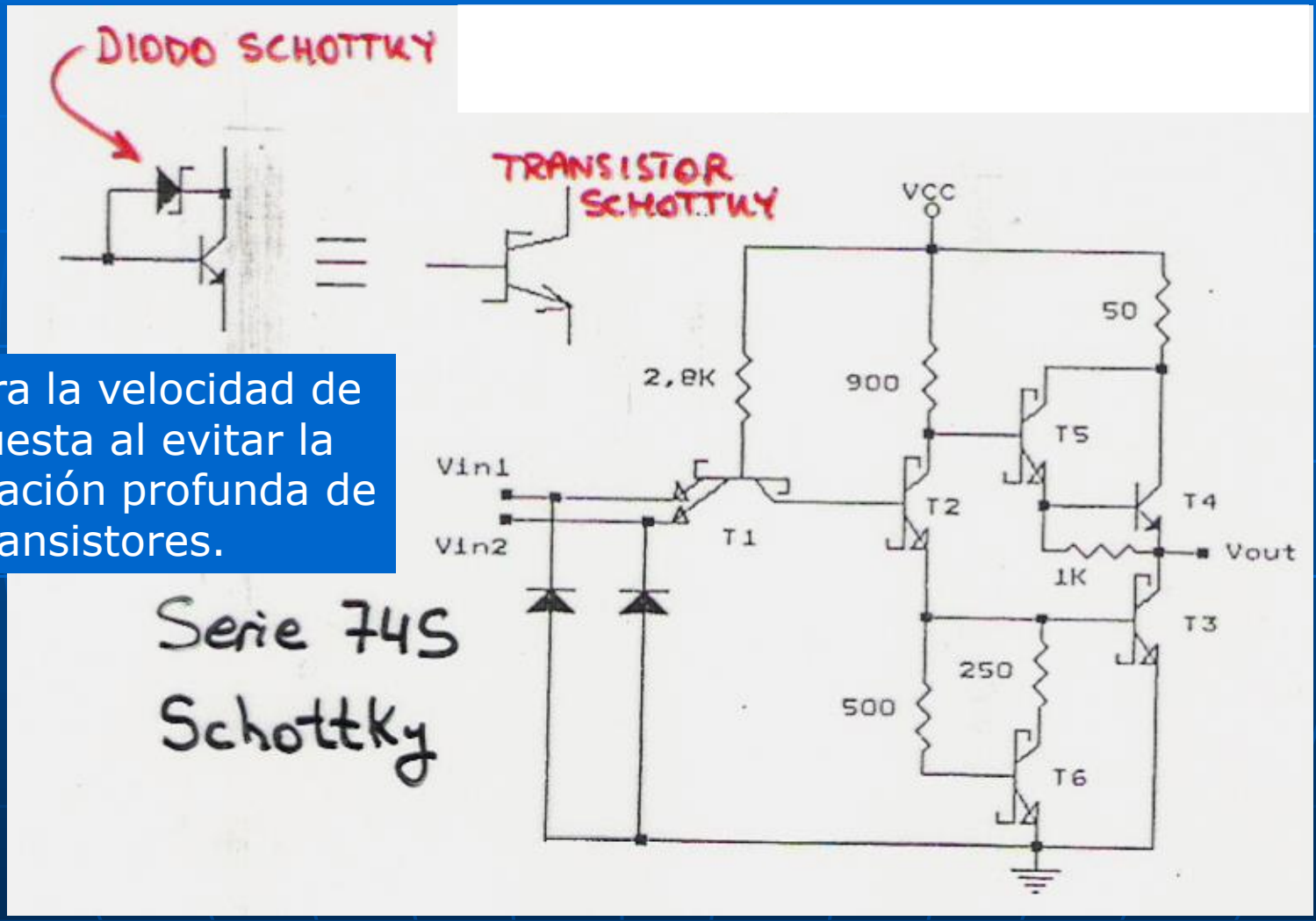
Lógica de tercer estado (tri-state)



Su función es de gran utilidad en los circuitos de interconexión entre un microprocesador con periféricos ya que estos últimos deben compartir el mismo bus de datos del micro y sólo uno debe estar activo en un dado momento.

Familias Lógicas

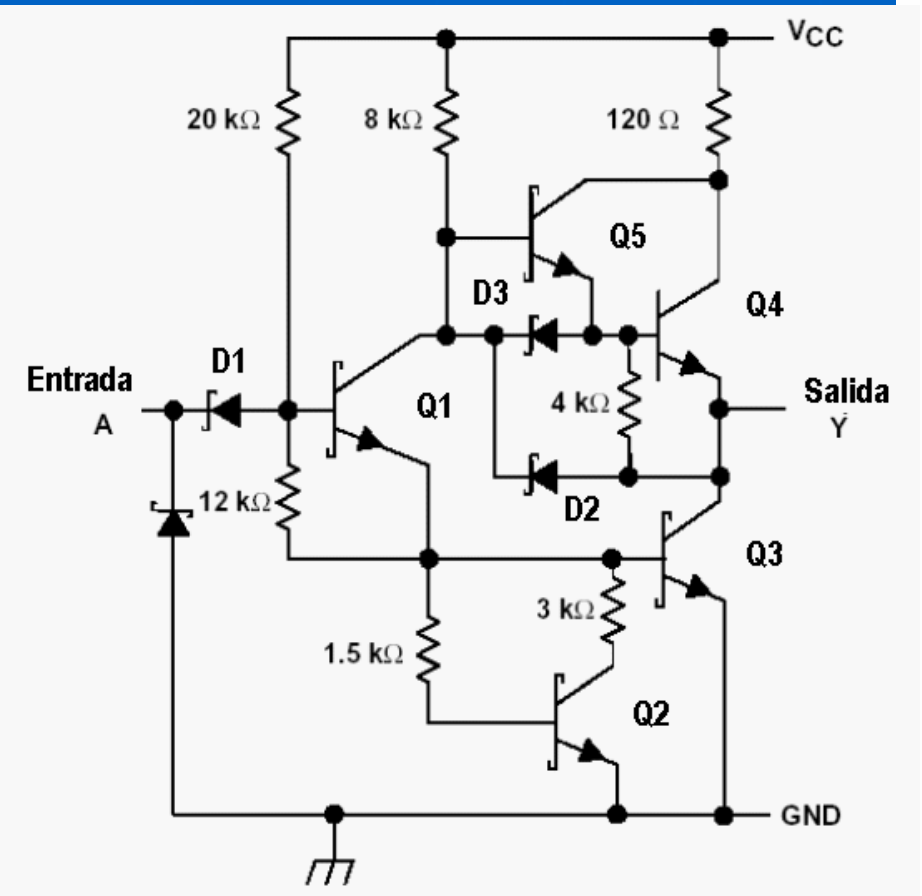
Tecnología TTL basada en el empleo de transistores Schottky

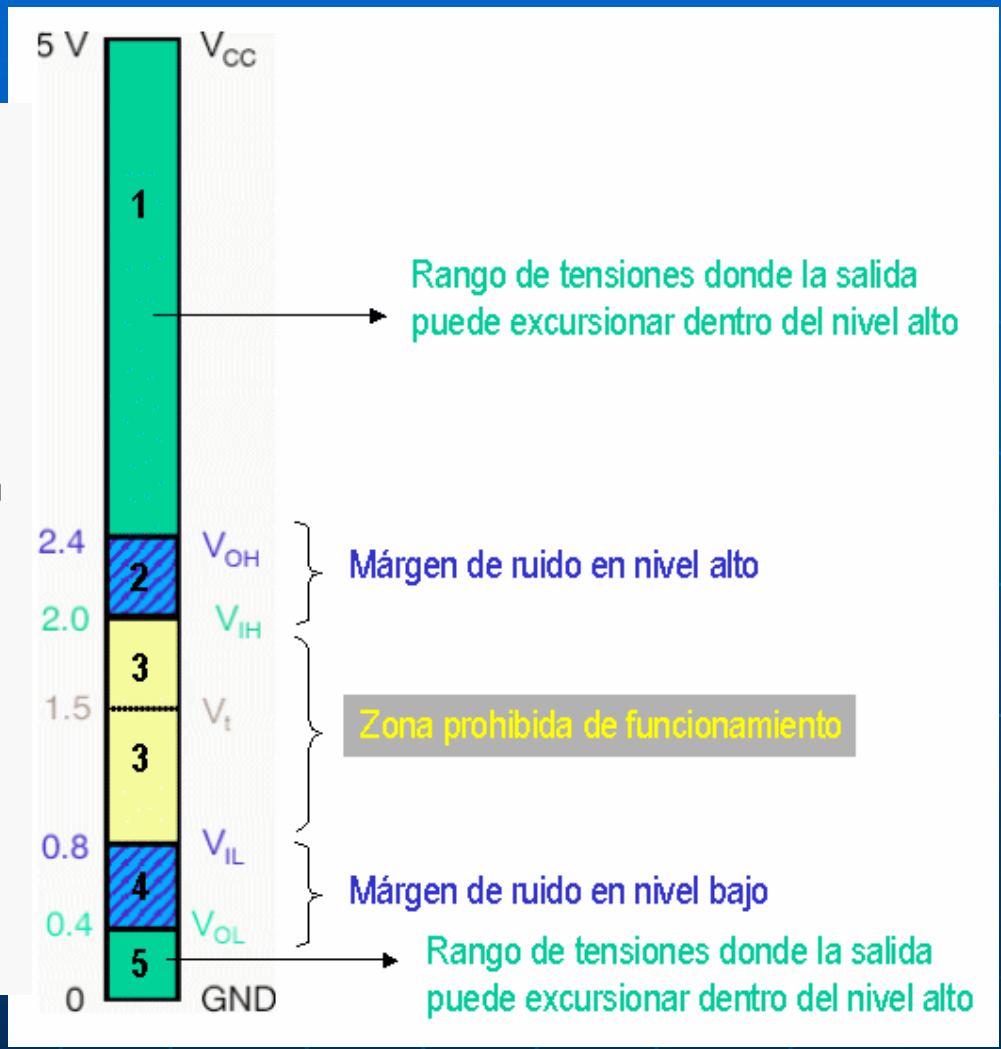


Mejora la velocidad de respuesta al evitar la saturación profunda de los transistores.

Familias Lógicas

Circuito de un inversor TTL serie 74 LS





Familias Lógicas

Familia TTL serie 74LS Características Generales

General Characteristics for Schottky TTL Logic (All Maximum Ratings)

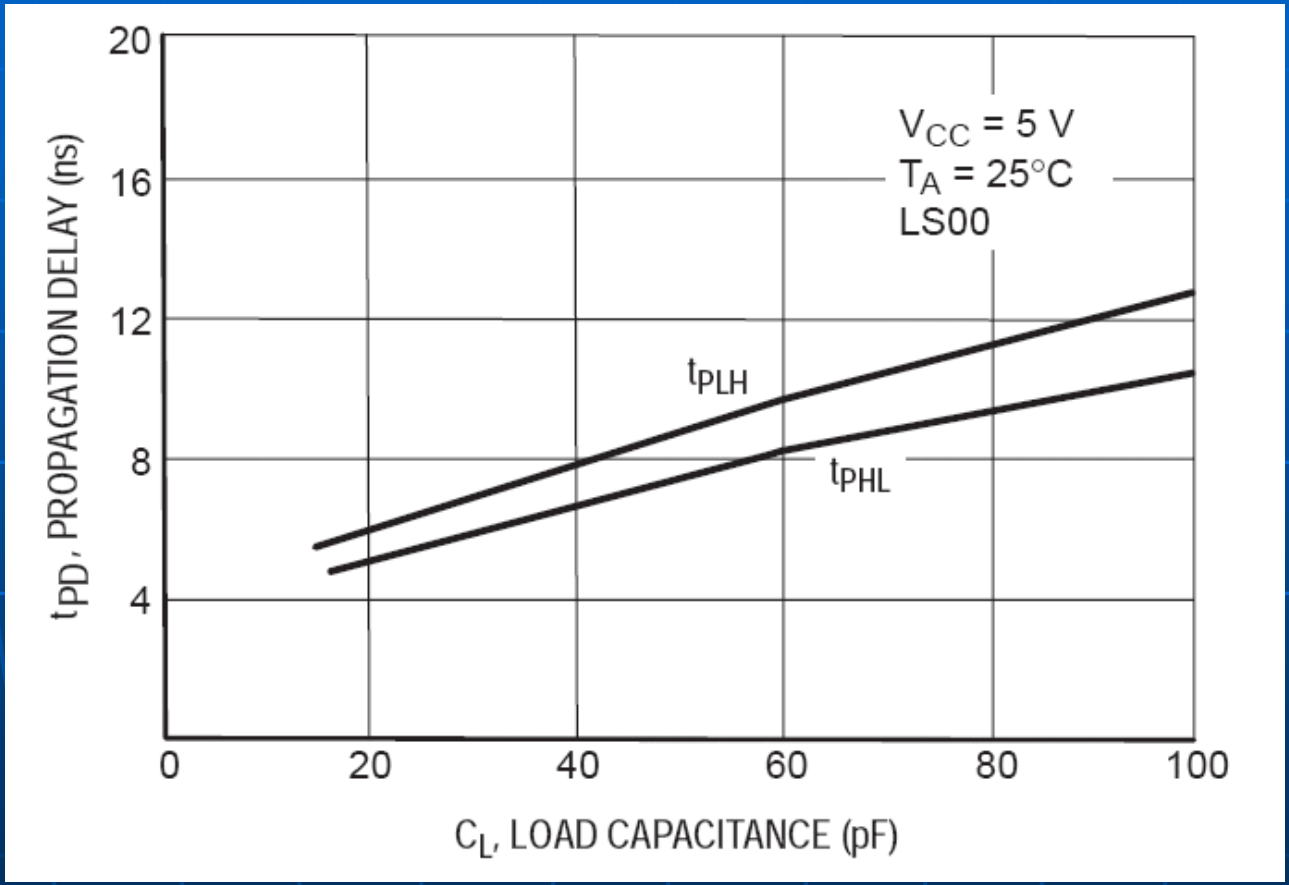
Characteristic	Symbol		74LSxxx	Unit
Operating Voltage Range	V_{CC}		5 ± 5%	Vdc
Operating Temperature Range	T_A		0 to 70	°C
Input Current	I_{IN}	I_{IH}	20	µA
		I_{IL}	−400	
Output Drive	I_{OH}		−0.4	mA
Standard Output	I_{OL}		8.0	mA
	I_{SC}		−20 to −100	mA
Buffer Output	I_{OH}		−15	mA
	I_{OL}		24	mA
	I_{SC}		−40 to −225	mA

Speed/Power Characteristics for Schottky TTL Logic(1) (All Typical Ratings)

Characteristic	Symbol	Typ	Unit
Quiescent Supply Current/Gate	I_G	0.4	mA
Power/Gate (Quiescent)	P_G	2.0	mW
Propagation Delay	t_p	9.0	ns
Speed Power Product	—	18	pJ
Clock Frequency (D-F/F)	f_{max}	33	MHz
Clock Frequency (Counter)	f_{max}	40	MHz

NOTES: 1. Specifications are shown for the following conditions:
a) V_{CC} = 5.0 Vdc (AC),
b) T_A = 25°C,
c) C_L = 15 pF.

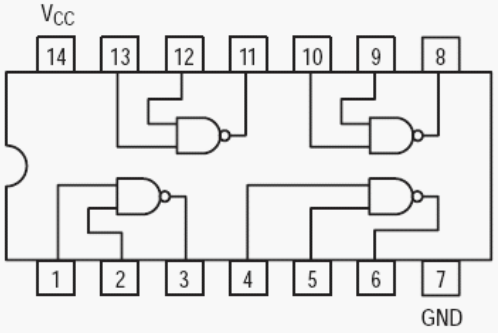
Familia TTL serie 74LS – Retardo de propagación vs. Capacidad de carga



SN74LS00

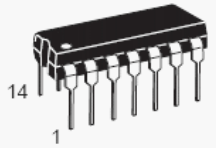
Quad 2-Input NAND Gate

- ESD > 3500 Volts



ON Semiconductor
Formerly a Division of Motorola
http://onsemi.com

LOW POWER SCHOTTKY



PLASTIC
N SUFFIX
CASE 646

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High			–0.4	mA
I_{OL}	Output Current – Low			8.0	mA

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH}	Turn–Off Delay, Input to Output		9.0	15	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL}	Turn–On Delay, Input to Output		10	15	ns	

SN74LS74A

Dual D-Type Positive Edge-Triggered Flip-Flop

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
f_{MAX}	Maximum Clock Frequency	25	33		MHz	Figure 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Clock, Clear, Set to Output		13	25	ns	Figure 1	
			25	40	ns		

AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
$t_{W(H)}$	Clock	25			ns	Figure 1	V_{CC} = 5.0 V
$t_{W(L)}$	Clear, Set	25			ns	Figure 2	
t_s	Data Setup Time — HIGH	20			ns	Figure 1	
	LOW	20			ns		
t_h	Hold Time	5.0			ns	Figure 1	

CONTADORES BCD Y BINARIO

SN74LS161A SN74LS163A

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f_{MAX}	Maximum Clock Frequency	25	32		MHz	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay Clock to TC		20 18	35 35	ns	
t_{PLH} t_{PHL}	Propagation Delay Clock to Q		13 18	24 27	ns	
t_{PLH} t_{PHL}	Propagation Delay CET to TC		9.0 9.0	14 14	ns	
t_{PHL}	$\overline{MR}$ or $\overline{SR}$ to Q		20	28	ns	

AC SETUP REQUIREMENTS (T_A = 25°C)

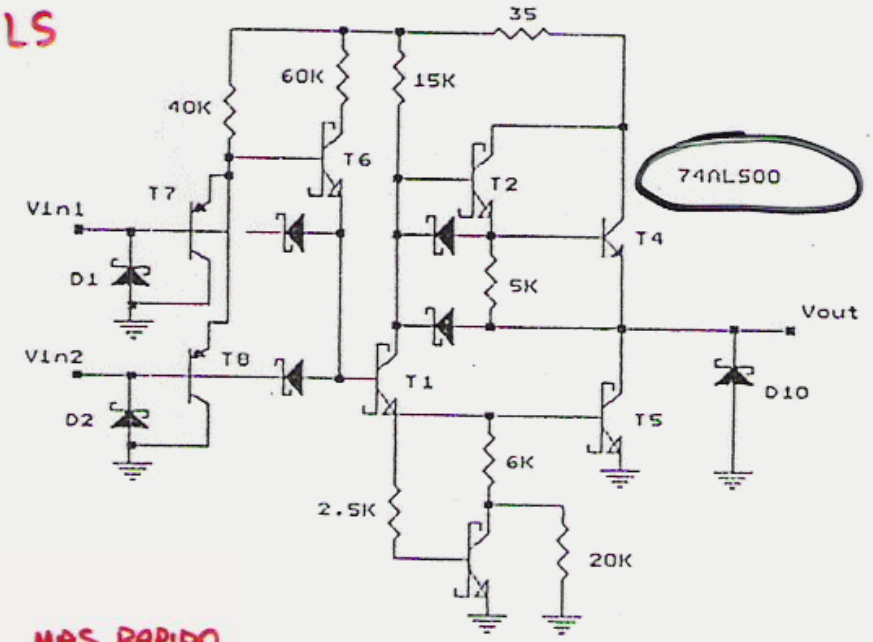
Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_WCP	Clock Pulse Width Low	25			ns	V_{CC} = 5.0 V
t_W	$\overline{MR}$ or $\overline{SR}$ Pulse Width	20			ns	
t_s	Setup Time, other*	20			ns	
t_s	Setup Time $\overline{PE}$ or $\overline{SR}$	25			ns	
t_h	Hold Time, data	3			ns	
t_h	Hold Time, other	0			ns	
t_{rec}	Recovery Time $\overline{MR}$ to CP	15			ns	

*CEP, CET, or DATA

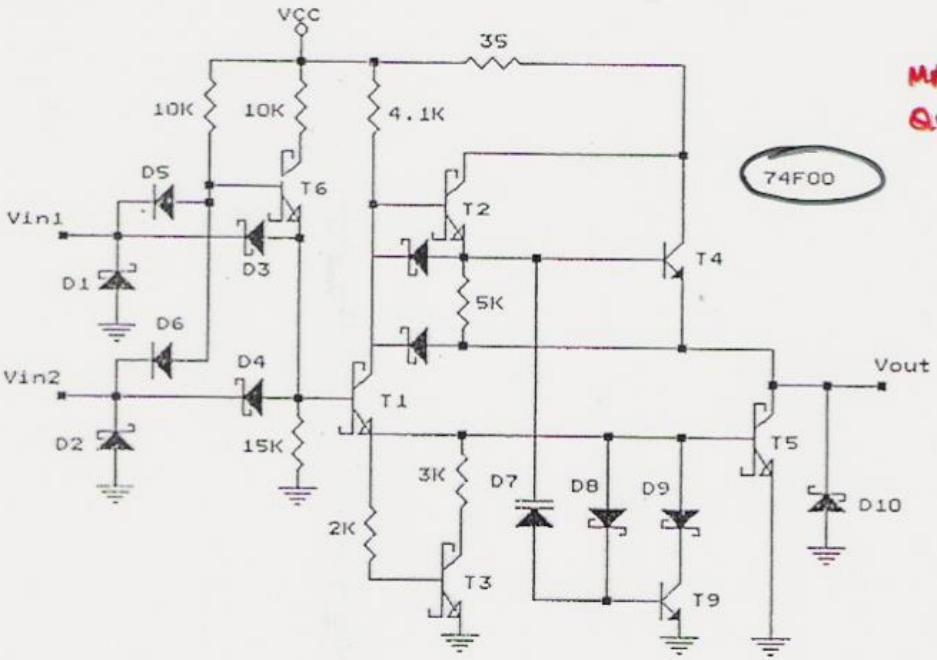
Familias Lógicas

FAMILIA TTL

MAS RAPIDO QUE LS
MAYOR MNoise



NAND de 2 entradas ALS



MAS RAPIDO QUE ALS

NAND de 2 entradas FAST

Familias Lógicas

FAMILIA TTL

Tabla de comparación entre subfamilias TTL

TTL Family Comparisons

General Characteristics for Schottky TTL Logic

(ALL MAXIMUM RATINGS)		LS		ALS			FAST		
Characteristic	Symbol	54LSxxx	74LSxxx	54ALSxxx	74ALSxxx		54Fxxx	74Fxxx	Units
Operating Voltage Range	V_{CC}	5 ± 10%	5 ± 5%	5 ± 10%	5 ± 10%	5 ± 5%	5 ± 10%	5 ± 5%	Vdc
Operating Temperature Range	T_A	- 55 to 125	0 to 70	- 55 to 125	0 to 70	0 to 70	55 to 125	0 to 70	°C
Input Current	I_{IN} I_{IH}	20	20	20	20	20	20	20	µA
	I_{IL}	- 400	- 400	- 100	- 100	- 100	- 600	- 600	
Output Drive	I_{OH}	- 0.4	- 0.4	- 0.4	- 0.4	- 0.4	- 1.0	- 1.0	mA
Standard Output	I_{OL}	4.0	8.0	4.0	8.0	8.0	20	20	mA
	I_{SC}	- 20 to - 100	- 20 to - 100	- 25 to - 150	- 25 to - 150	- 25 to - 150	- 60 to - 150	- 60 to - 150	mA
Buffer Output	I_{OH}	- 12	- 15	- 12	- 15	- 15	- 12	- 15	mA
	I_{OL}	12	24	12	24	24	48	64	mA
	I_{SC}	- 40 to - 225	- 40 to - 225	- 50 to - 225	- 50 to - 225	- 50 to - 225	- 100 to - 225	- 100 to - 225	mA
Buffer Line Driving Capability: Minimum R_L into 2.5 V		178	84	178	84	84	43	32	Ω
Minimum R_L into 5.0 V		381	189	381	189	189	95	71	Ω

Familias Lógicas

Tabla de comparación entre subfamilias TTL

Speed/Power Characteristics for Schottky TTL Logic(1)

(ALL TYPICAL RATINGS)

Characteristic	Symbol	LS	ALS	FAST	Units
Quiescent Supply Current/Gate	I_G	0.4	0.2	1.1	mA
Power/Gate (Quiescent)	P_G	2.0	1.0	5.5	mW
Propagation Delay	t_p	9.0	5.0	3.7	ns
Speed Power Product	—	18	5.0	19.2	pJ
Clock Frequency (D-F/F)	f_{max}	33	35	125	MHz
Clock Frequency (Counter)	f_{max}	40	45	125	MHz

La serie FAST (74F)es la subfamilia más rápida TTL pero también de mas consumo.
Le sigue la ALS (74ALS) y luego por último la LS (74LS).
La mas popular y económica que todavía sigue consiguiéndose con facilidad a precio bajo es la LS.

Lógica CMOS

Evolución:

Serie 4000, serie 4000UB-4000B,
Serie 74C, serie 74HC-74HCT, serie 74AC-74ACT,
Serie 74AHC-74AHCT, etc..
Versiones de baja tensión de alimentación.

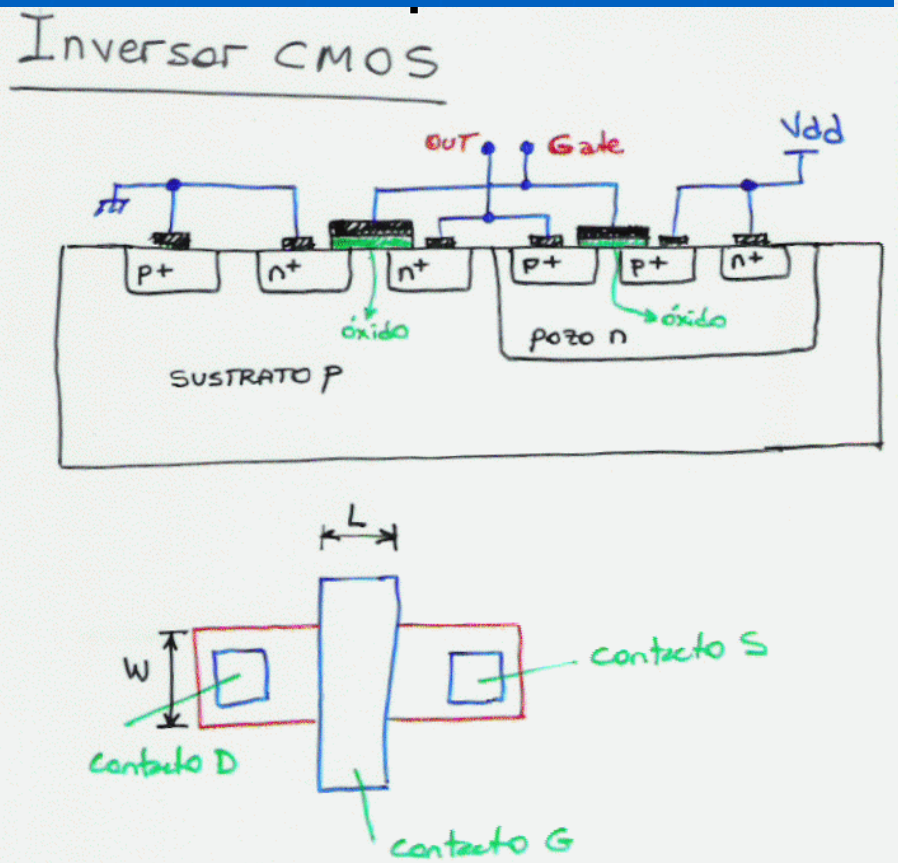
Lógica CMOS

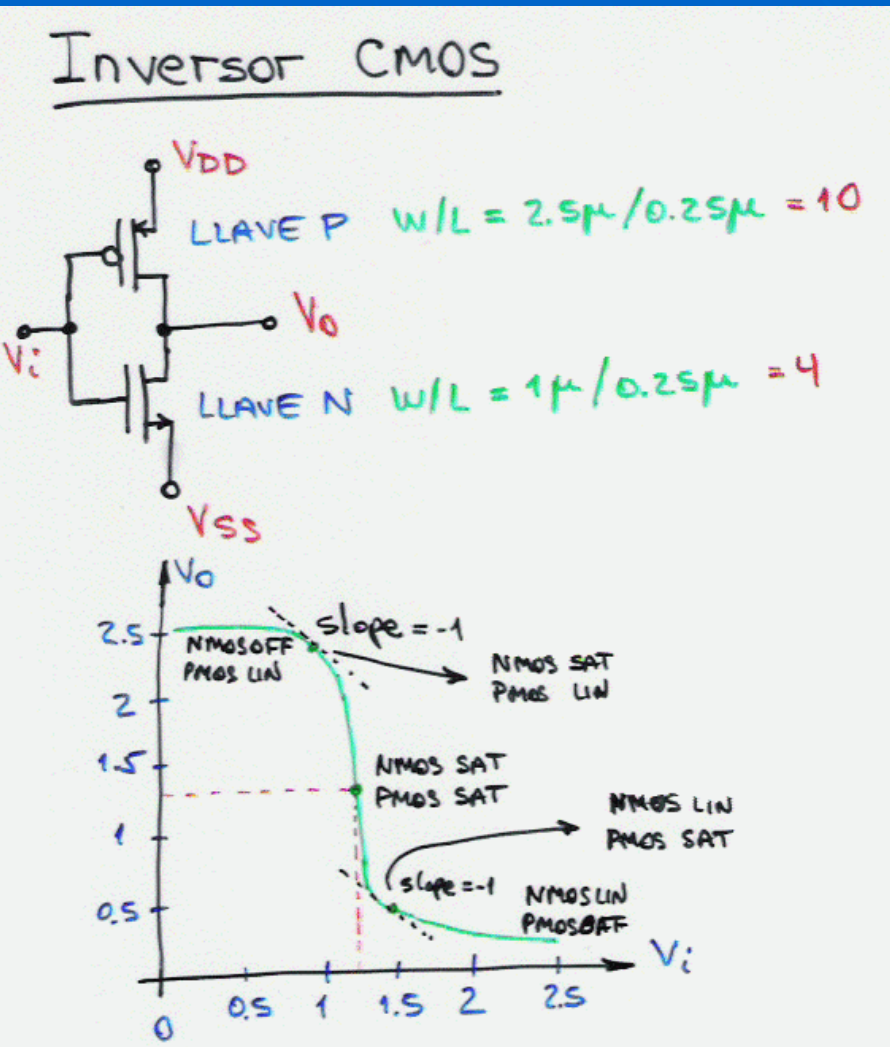
Serie 4000

Es la mas antigua de CMOS.
Sus mayores ventajas son:
Extremado bajo consumo.
Alta inmunidad al ruido.
Alto Fan-out.
Rango de tensiones de alimentación amplio (3 V a 18V).
Principal desventaja: Velocidad.

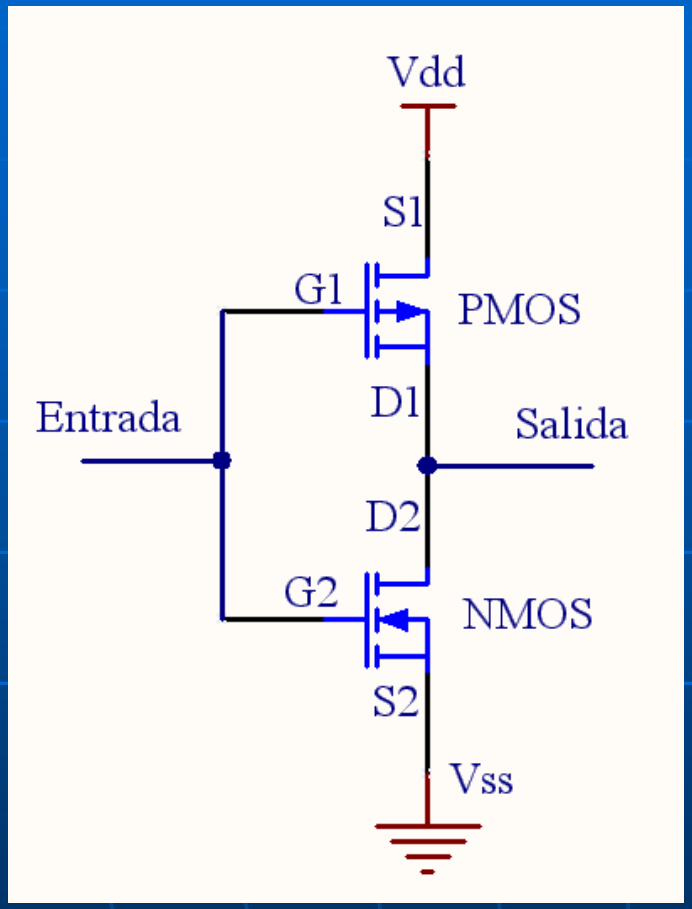
En la actualidad viene en dos versiones: 4xxxUB y 4xxxB.
La primera, UB (unbuffered) es mas rápida pero con poca capacidad de corriente de salida.
La segunda, B (buffered) es mas lenta pero tiene mayor corriente para alimentar cargas TTL ya que posee un driver a la salida (generalmente un inversor) con lo cual hay que negar dos veces y eso hace mas lento al circuito.

Circuito de un inversor CMOS

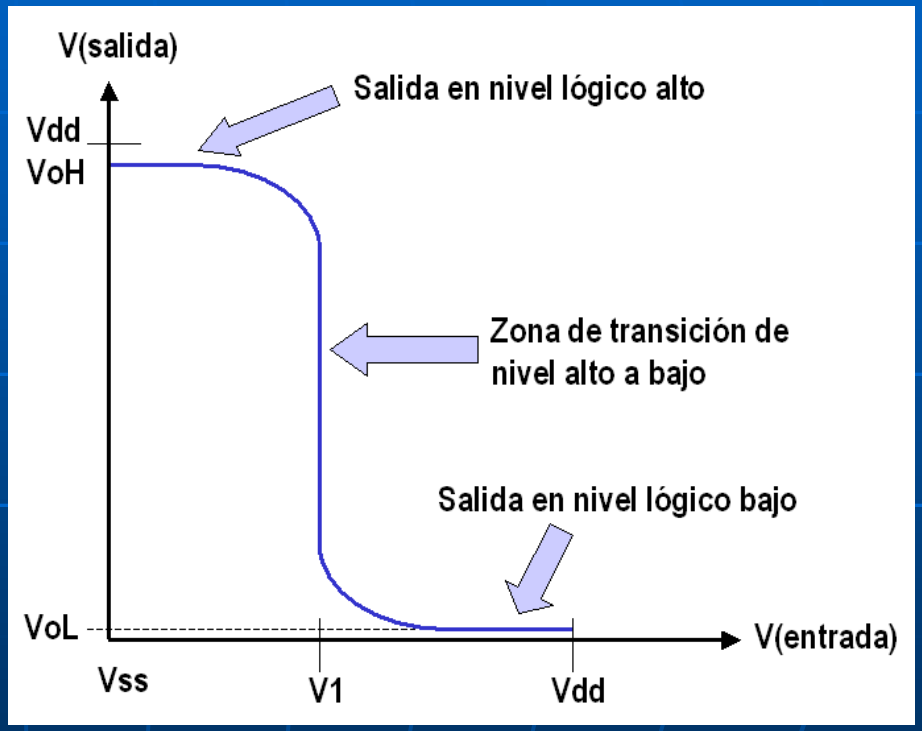




Circuito de un inversor CMOS

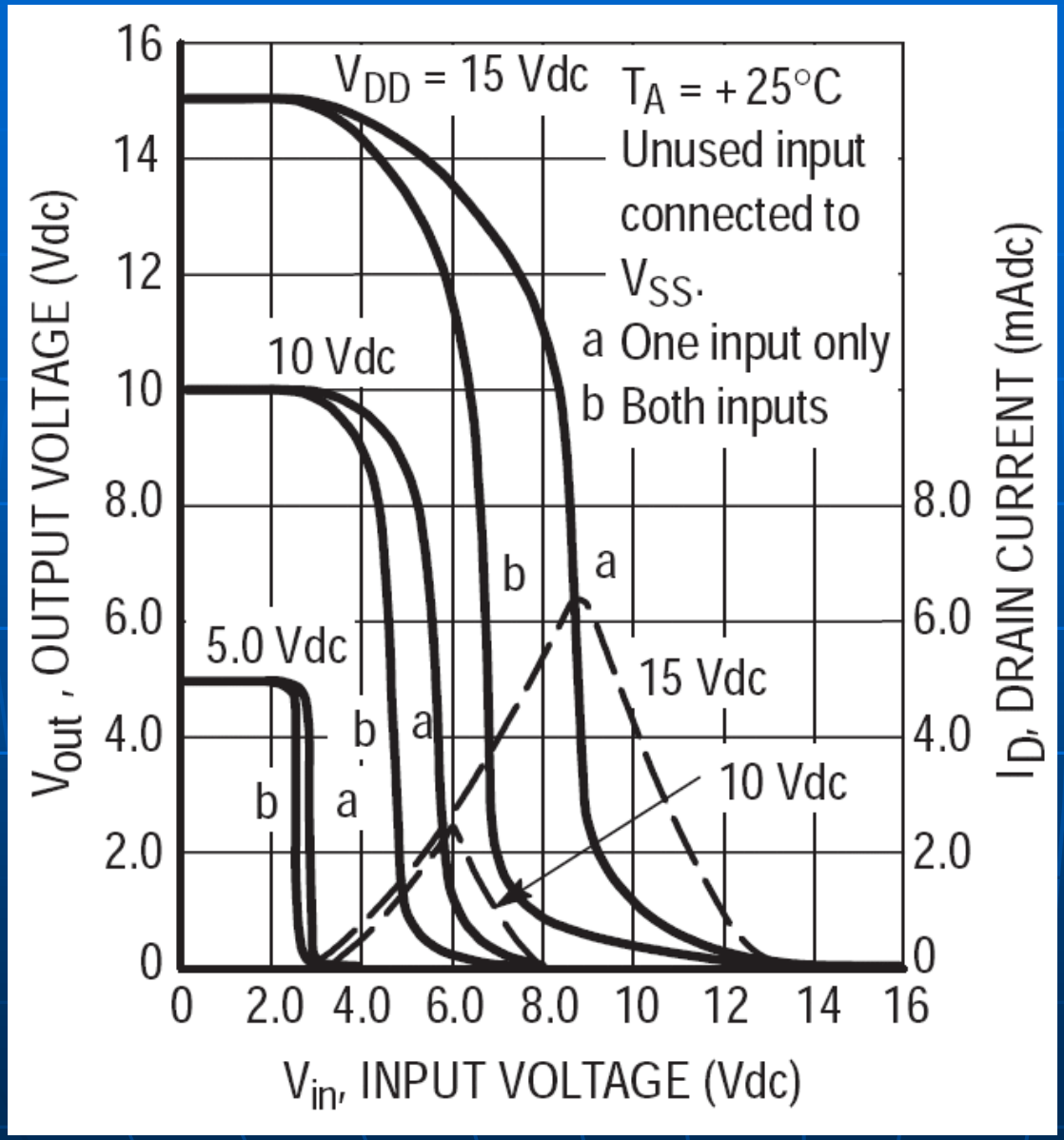


Respuesta idealizada



Familias Lógicas

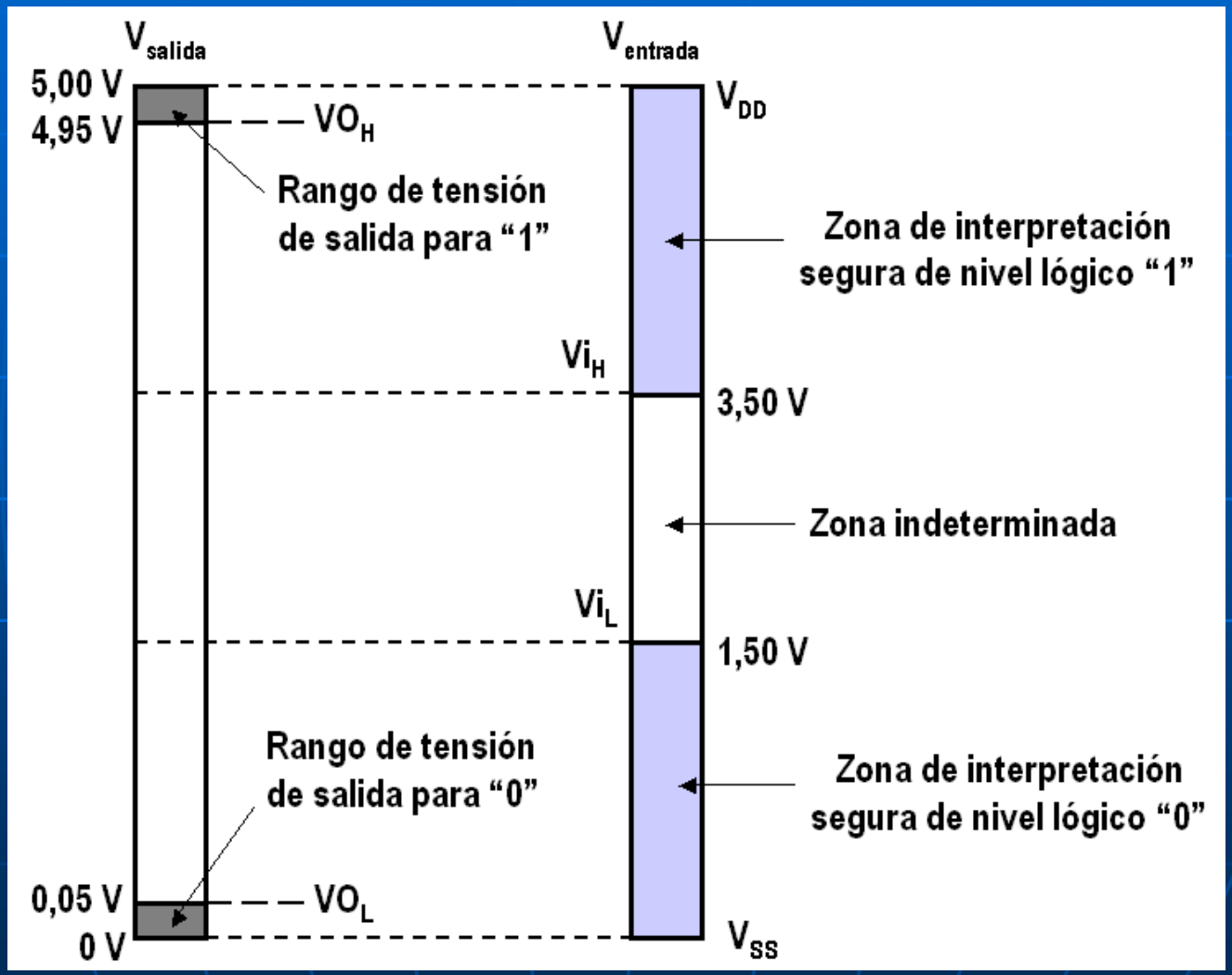
FAMILIA CMOS



FUNCIÓN DE TRANSFERENCIA REAL DE HOJAS DE DATOS DE ALGUNAS COMPUERTAS CMOS SERIE 4000 para 3 niveles de tensión de alimentación Vdd: 5, 10 y 15 V y con temperatura ambiente estable en 25ºC.

Qué funciones lógicas puede representar este tipo de respuesta …??

Márgen de ruido en CMOS



Ecuaciones del MOSFET canal N

- **Región de corte:** $I_{ds} = 0$ para $V_{gs} - V_T < 0$
- **Región lineal:**

$$I_{ds} = \mu C_{ox} \cdot \frac{W}{L} \cdot \left[(V_{gs} - V_T) \cdot V_{ds} - \frac{V_{ds}^2}{2} \right] \cdot (1 + \lambda \cdot V_{ds})$$

para $0 < V_{ds} < V_{gs} - V_T$

- Capacidad del óxido

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \ (F/m^2)$$

→ espesor

- **Región de saturación:**

$$I_{ds} = \frac{\mu C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{gs} - V_T)^2 \cdot (1 + \lambda V_{ds}) \quad \text{para} \quad V_{ds} > V_{gs} - V_T$$

Retardo de propagación

$$t_{PLH} = \frac{C_L \cdot V_{dd}}{k_p (V_{dd} - |V_{TP}|)^2} \simeq \frac{C_L}{k_p \cdot V_{dd}}$$

$k_p \propto 1/L_p$

$$t_{PHL} = \frac{C_L \cdot V_{dd}}{k_n (V_{dd} - |V_{TN}|)^2} \simeq \frac{C_L}{k_n \cdot V_{dd}}$$

$k_n \propto 1/L_n$

$$t_p \simeq \frac{1}{2}(t_{PLH} + t_{PLH}) = \frac{C_L}{2 \cdot V_{dd}} \cdot \left(\frac{1}{k_n} + \frac{1}{k_p}\right)$$

Para reducir retardos:

- REDUCIR C_L
- INCREMENTAR k_n y k_p
  $\Rightarrow$ aumentar $W/L \Rightarrow I_{DS} \uparrow$

Inversor CMOS

Disipación de potencia dinámica

- Función del tamaño del transistor (Capacidades de GATE y parásitas)
- Para reducir P_d se puede:
  - Reducir C_L
  - Reducir V_{dd} ⇒ MAS EFECTIVO
  - Reducir frec.

$$E = \frac{1}{2} C_L \cdot V_{dd}^2$$

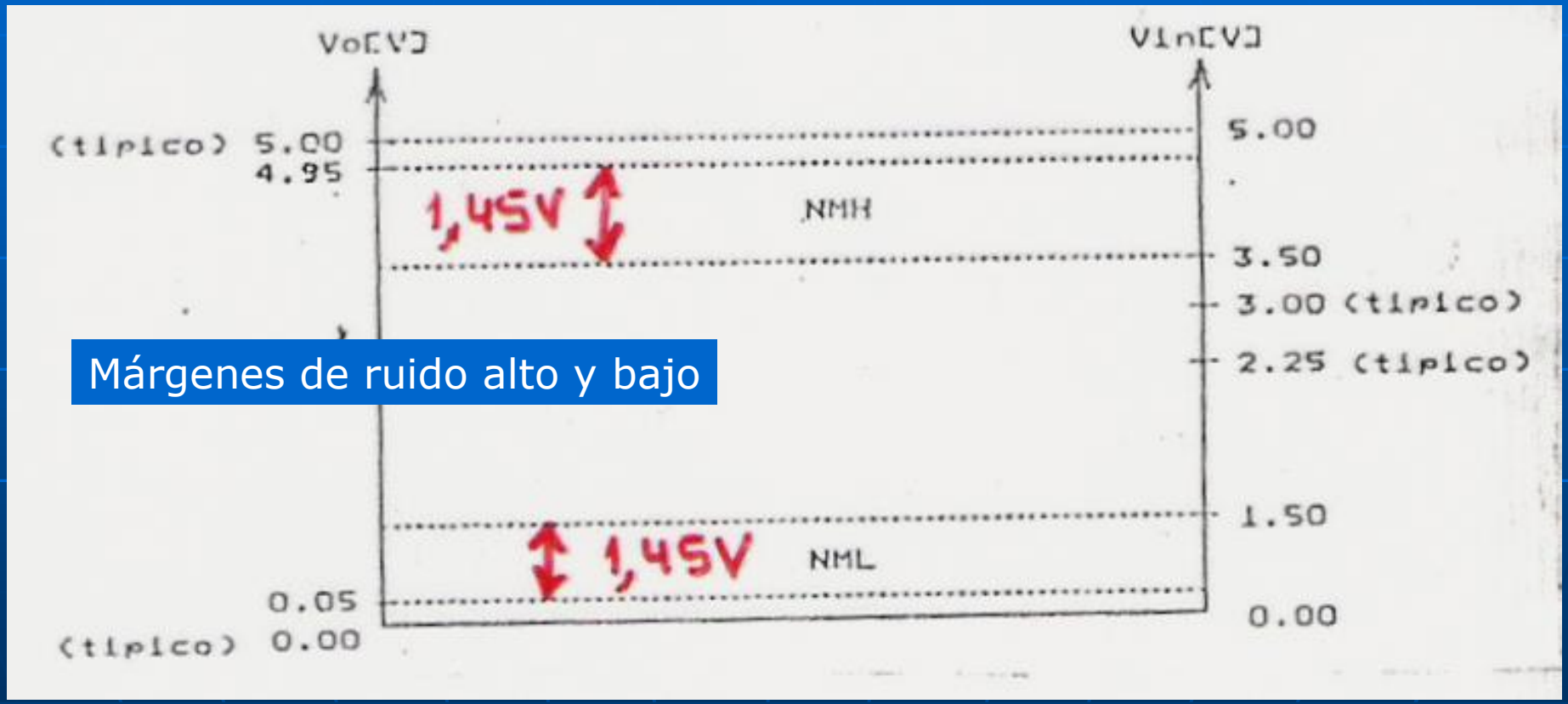
$$P = 2 \cdot f \cdot E = f \cdot C_L \cdot V_{dd}^2$$

Familias Lógicas

Márgenes de ruido en CMOS standard para 5 volts de alimentación

Salida de una compuerta

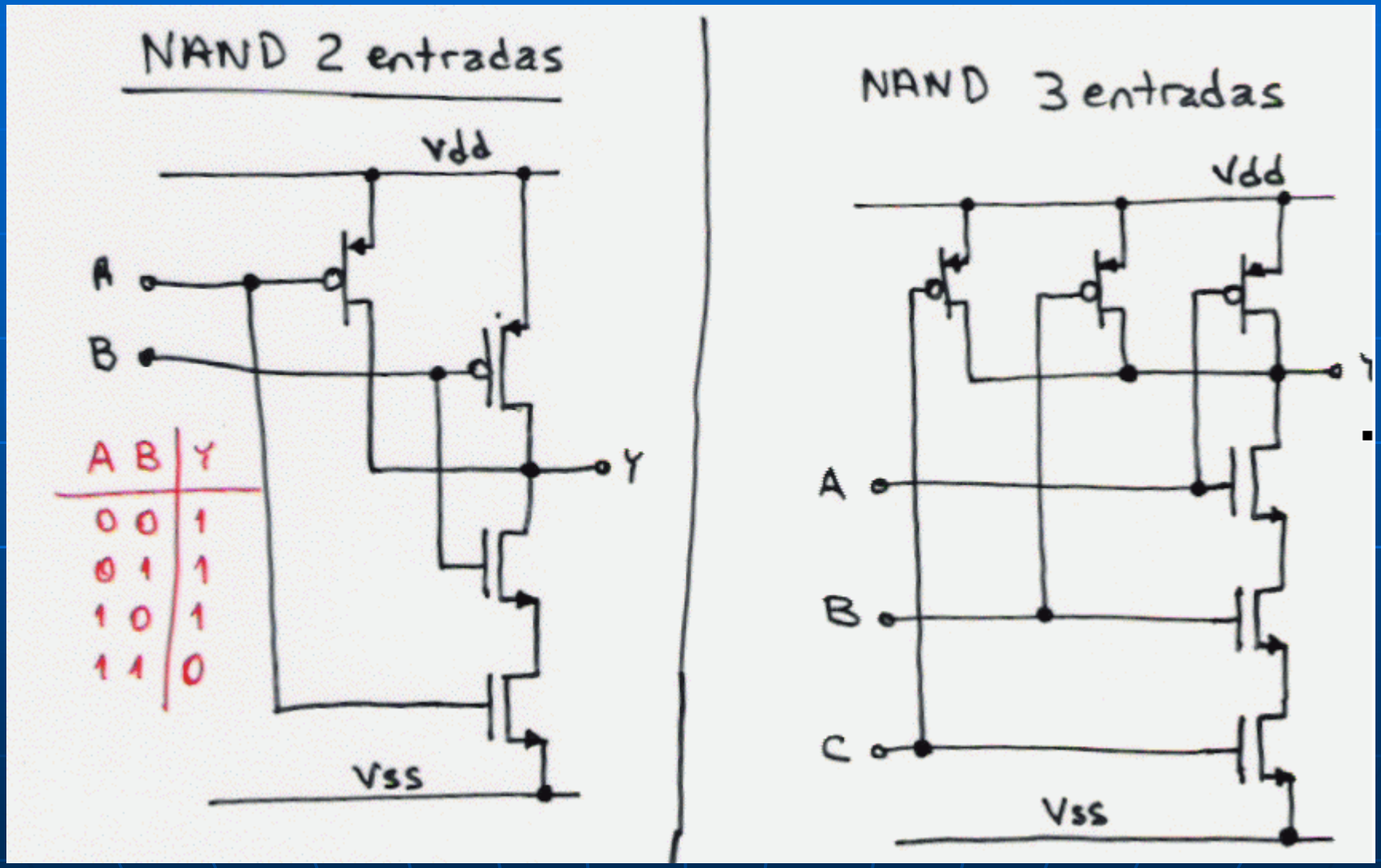
Entrada de otra compuerta



Márgenes de ruido alto y bajo

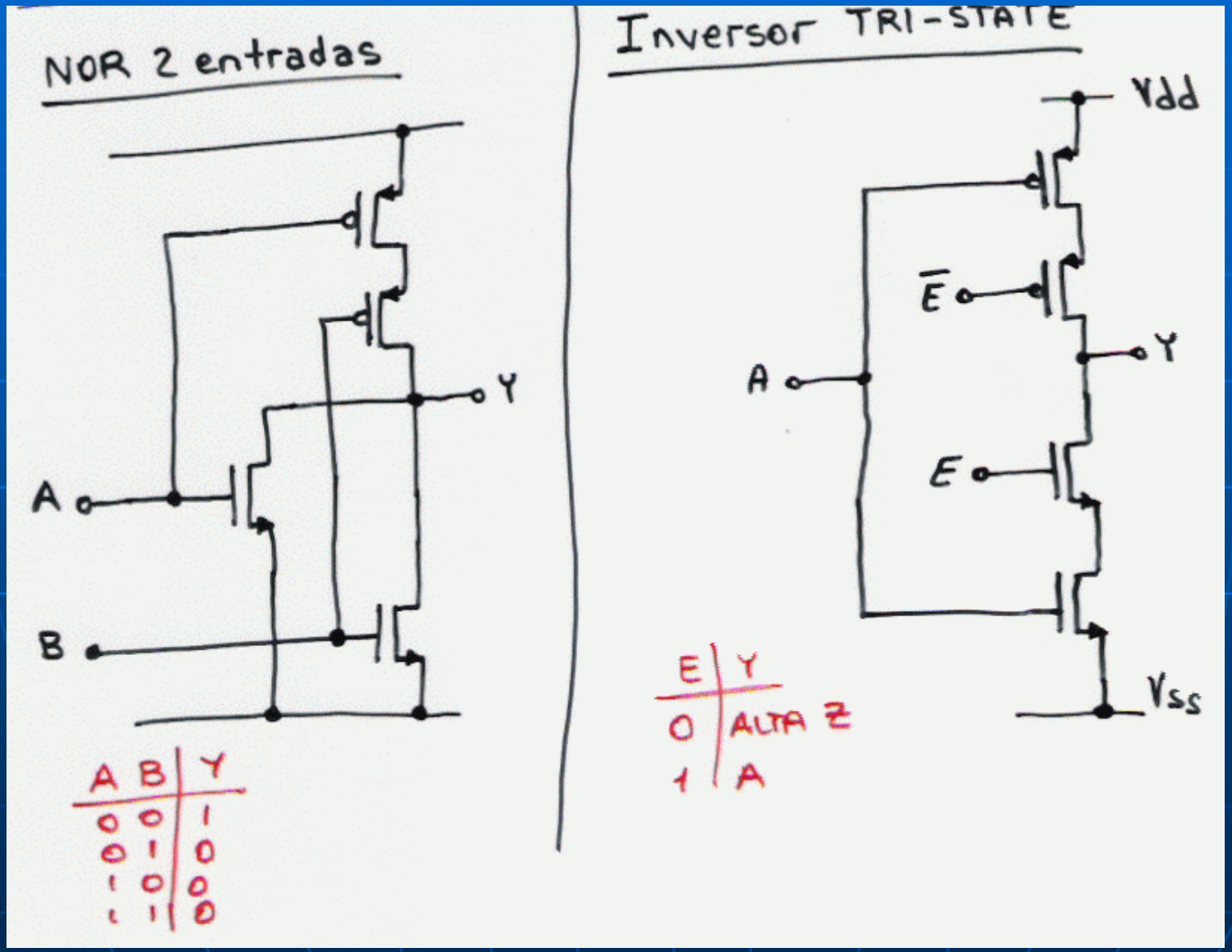
Familias Lógicas

Estructuras simples de compuertas CMOS (caso NAND)



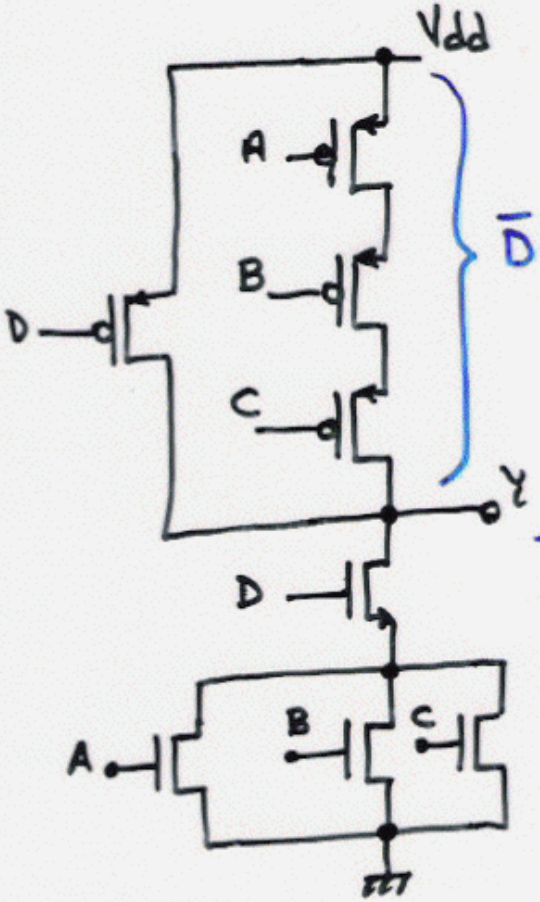
Familias Lógicas

Estructuras simples de compuertas CMOS (caso NOR y tercer estado)



Compuertas CMOS complejas

Función : $Y = \overline{D \cdot (A+B+C)}$

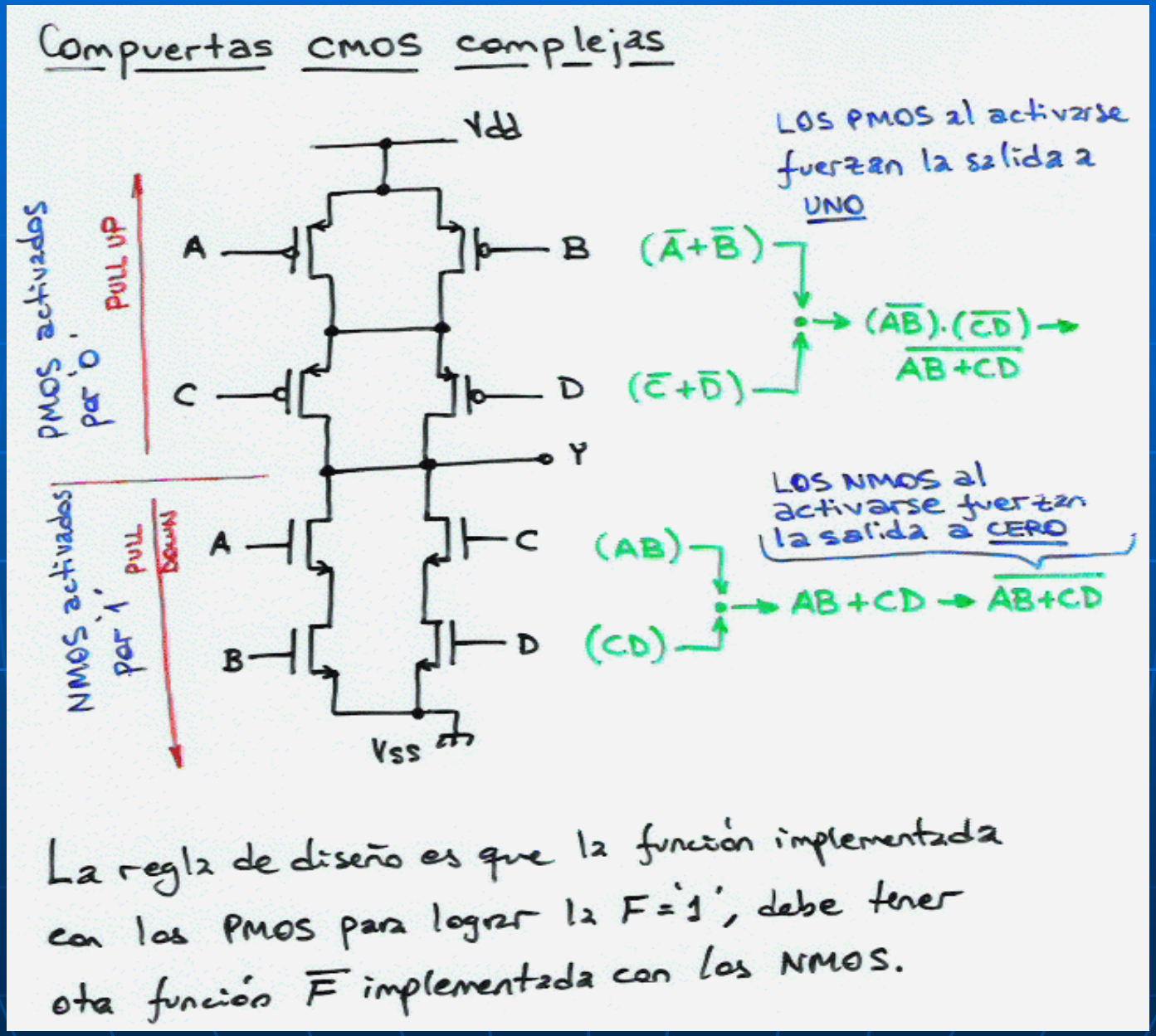


$\overline{D} + \overline{A}\,\overline{B}\,\overline{C} = Y = \overline{\overline{Y}} = \overline{D \cdot (A+B+C)}$

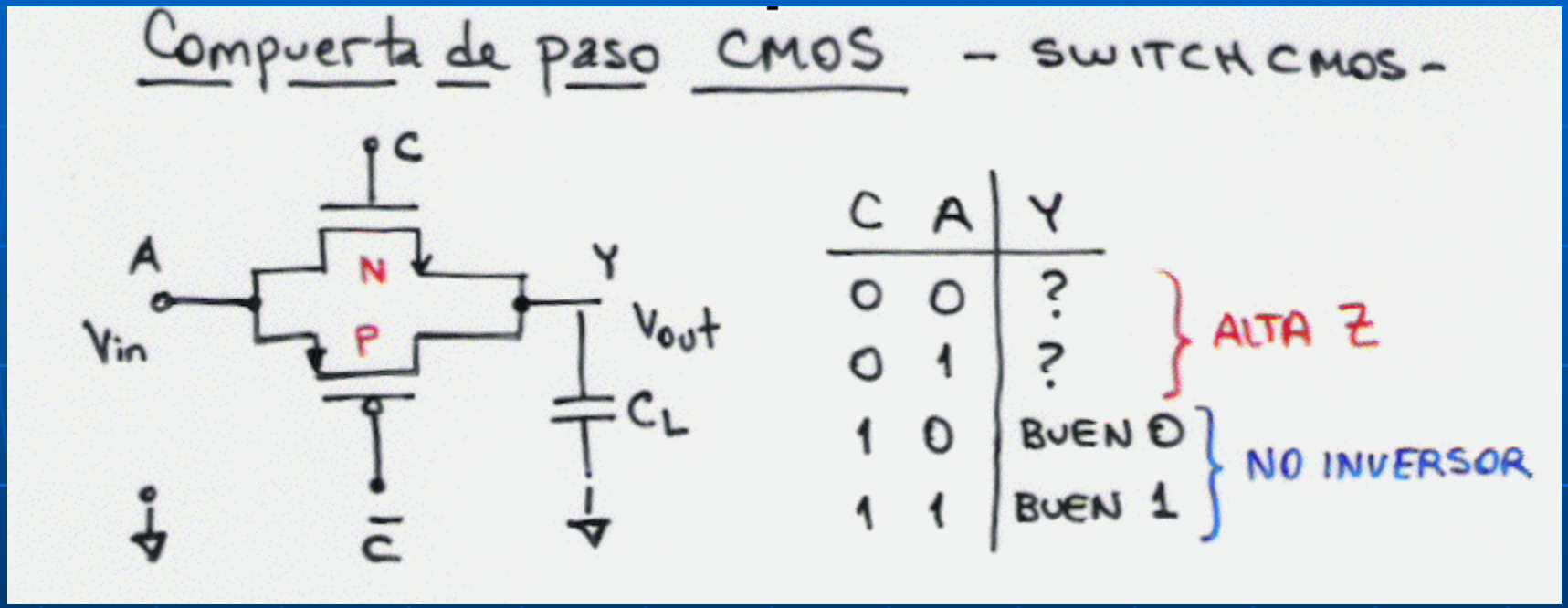
$= \overline{D} + \overline{(A+B+C)} = \overline{D} + \overline{A} \cdot \overline{B}\,\overline{C}$

$D \cdot (A+B+C) = \overline{Y}$

Ciertas funciones se pueden implementar con un solo bloque de retardos .
En TTL exigiría 3 niveles de compuertas ...!!!!!


Compuertas CMOS complejas
Vdd
A
B
C
D
Y
A
C
B
D
Vss
PMOS activados por '0'
PULL UP
NMOS activados por '1'
PULL DOWN
LOS PMOS al activarse fuerzan la salida a UNO
$(\bar{A}+\bar{B})$
$(\bar{C}+\bar{D})$
$(\overline{AB}).(\overline{CD}) \rightarrow \overline{AB+CD}$
LOS NMOS al activarse fuerzan la salida a CERO
(AB)
(CD)
$AB+CD \rightarrow \overline{AB+CD}$
La regla de diseño es que la función implementada con los PMOS para lograr la F='1', debe tener ota función $\bar{F}$ implementada con los NMOS.

Estructura Pass-gate (compuerta de paso)



Familias Lógicas

Funcionamiento de compuerta tipo pass-gate

Transición de entrada de 0 a 1

NMOS: trabaja como seguidor por fuente

$V_{gs} = V_{ds}$ siempre.

Cuando $V_{out} < V_{dd} - V_{tN}$ → SATURA

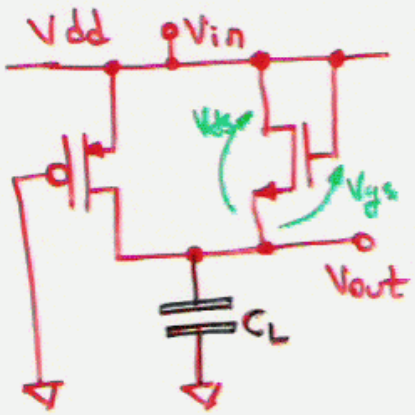
Cuando $V_{out} > V_{dd} - V_{tN}$ → CORTA

PMOS: trabaja como fuente de corriente

Cuando $V_{out} < |V_{tp}|$ → SATURA

Cuando $V_{out} > V_{tp}$ → FUNC. LINEAL

CIRCUITO EQUIVALENTE



Transición de entrada de 1 a 0

NMOS: trabaja como fuente de corriente

Cuando $V_{out} > V_{dd} - V_{tN}$ → SATURA

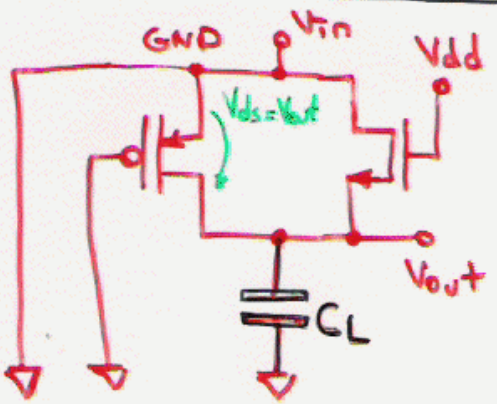
Cuando $V_{out} < V_{dd} - V_{tN}$ → FUNC. LIN.

PMOS: trabaja como seguidor por fuente

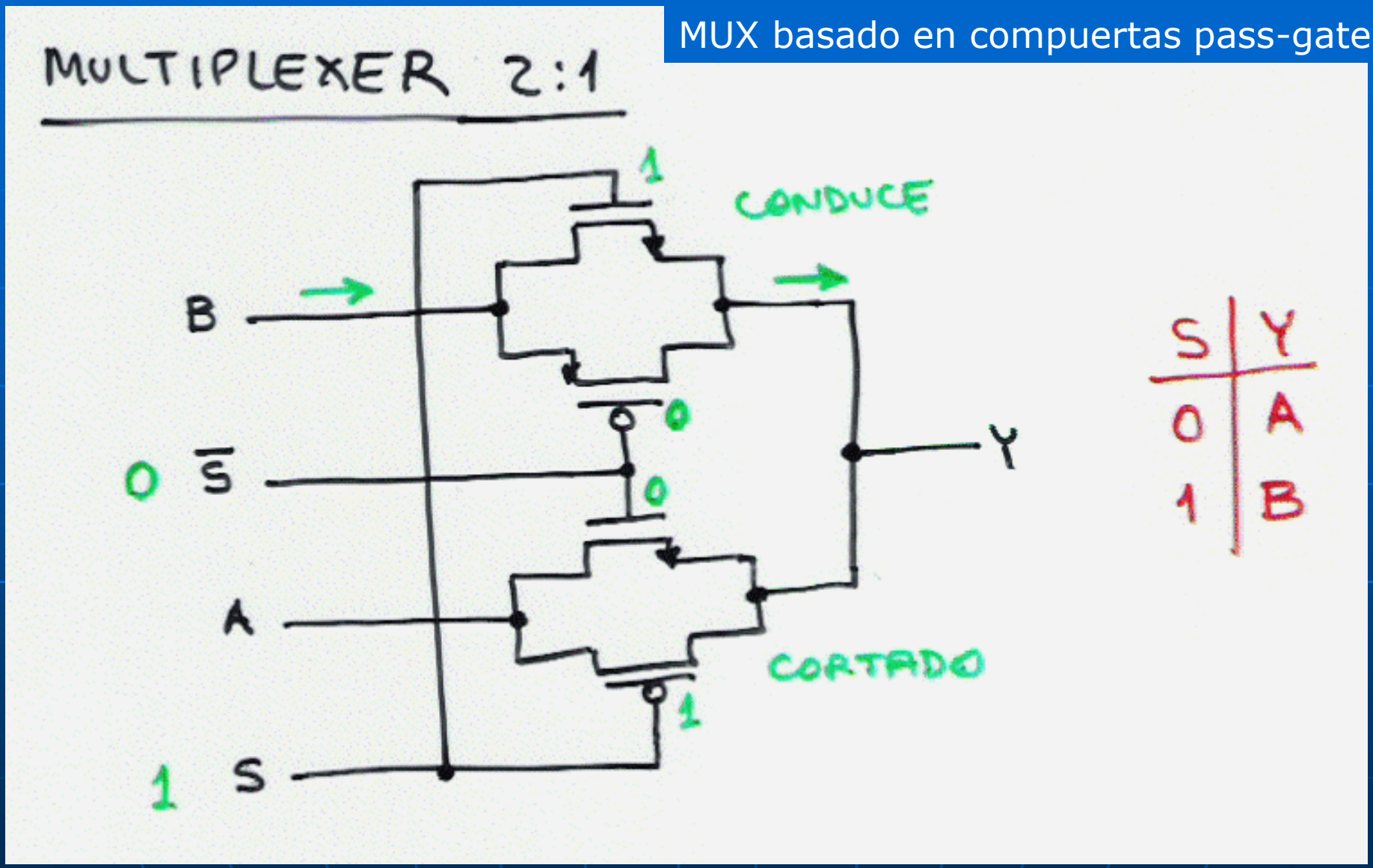
$V_{gs} = V_{ss}$ siempre

Cuando $V_{out} > |V_{tp}|$ → SATURA

Cuando $V_{out} < V_{tp}$ → CORTA



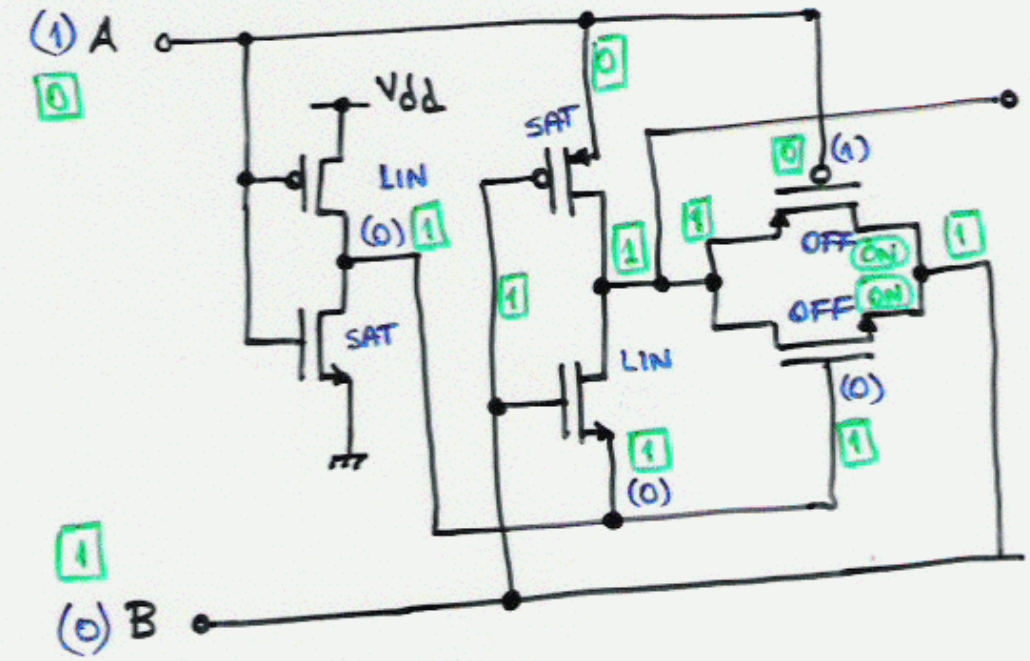
MUX basado en compuertas pass-gate



S	Y
0	A
1	B

OR EXCLUSIVA

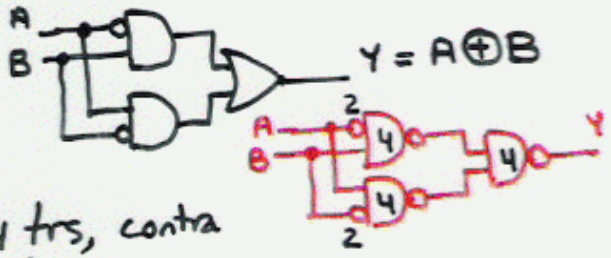
OR-EXCL basada en pass-gate



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

MAS SIMPLE, MENOR RETARDO QUE

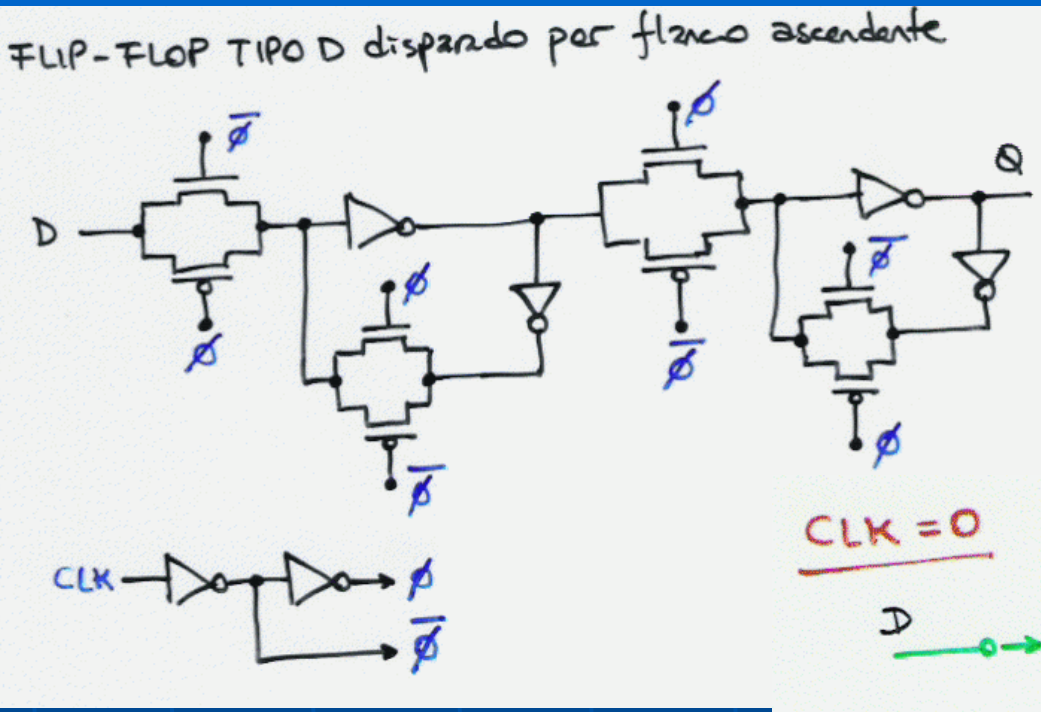
USANDO : A, B



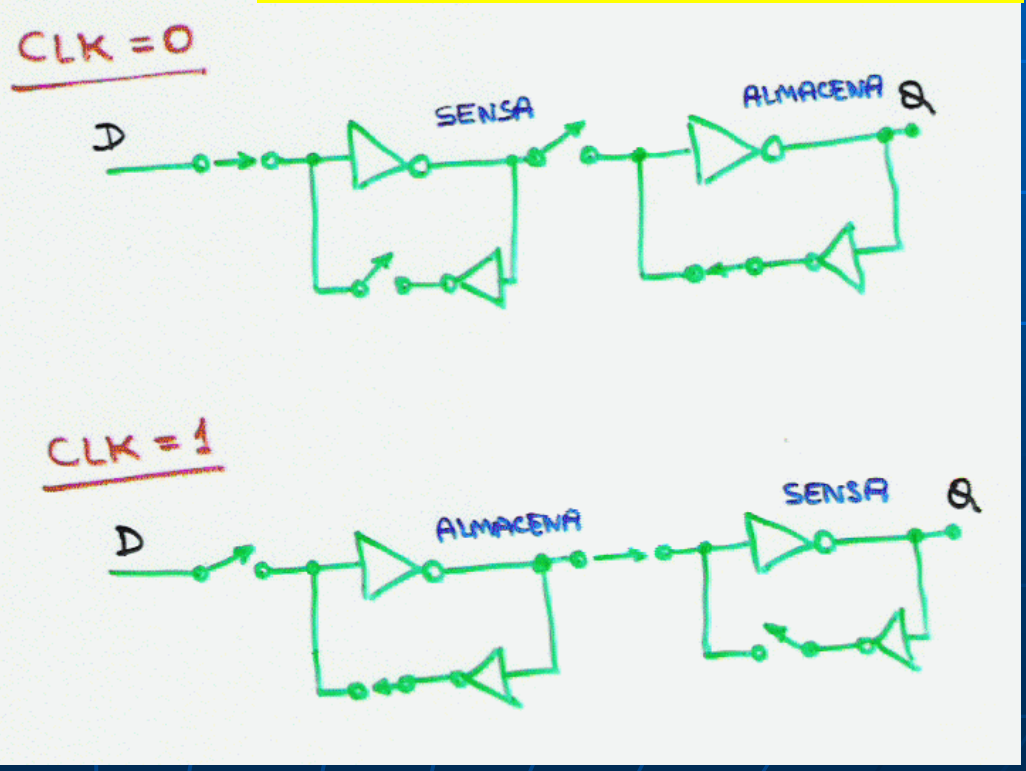
Total : 14 trs, contra 6 trs

Dado el muy bajo consumo se tiene la posibilidad de "colgar" compuertas alimentadas de otras. Esto permite por ejemplo hacer una Or-Exclusiva.

Familias Lógicas



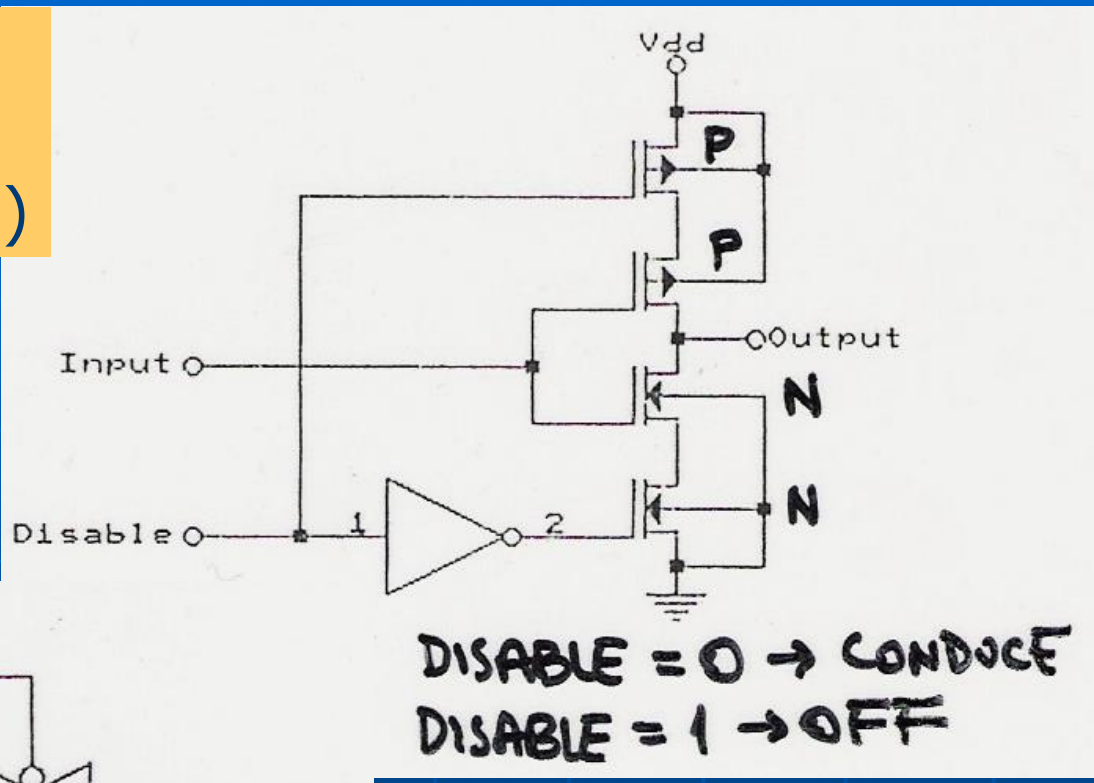
Implementación de un FF tipo "D" disparado por flanco ascendente.
Tiene una configuración tipo master-salve, es decir, dos bloques idénticos que se activan con niveles de tensión diferentes de CLK.

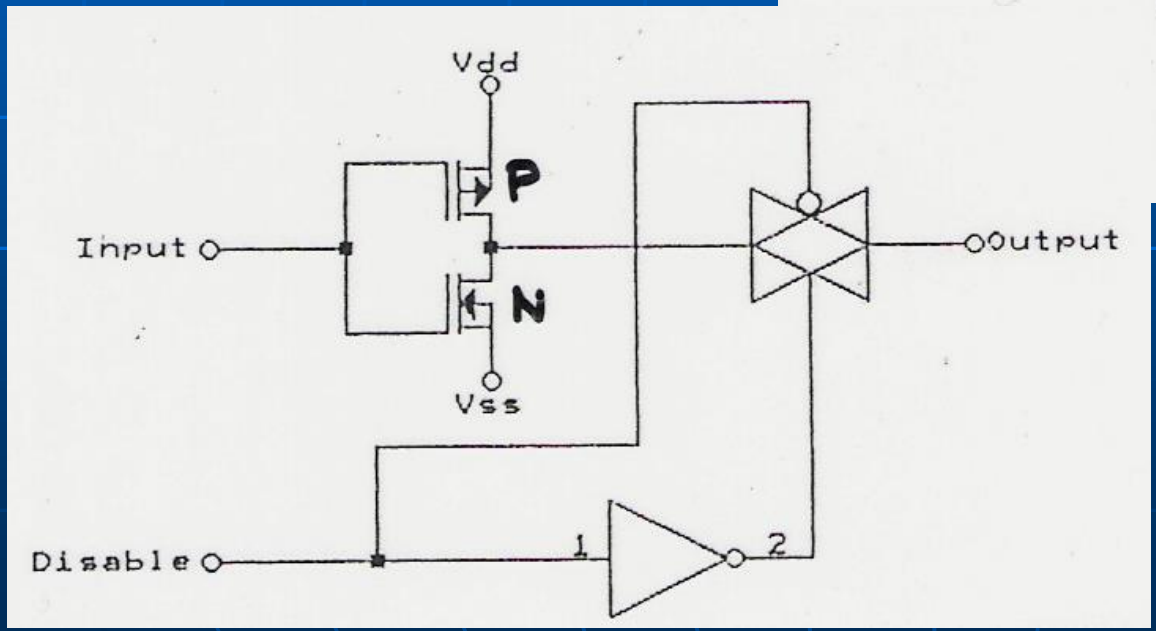


Cómo se puede hacer uno que sea sensible al otro flanco..??

Familias Lógicas

Dos posibilidades para lograr compuertas con tercer estado (tri-state)





Familias Lógicas

FAMILIA CMOS

Serie MC14001UB (unbuffered)

baja capacidad de corriente

MC14001UB, MC14011UB

UB-Suffix Series CMOS Gates

The UB Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired. The UB set of CMOS gates are inverting non–buffered functions.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linear and Oscillator Applications
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin–for–Pin Replacements for Corresponding CD4000 Series UB Suffix Devices

Familias Lógicas

Serie MC14001UB (unbuffered)

FAMILIA CMOS

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (3.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD} "1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 Vdc) (V_O = 9.0 Vdc) (V_O = 13.5 Vdc)		5.0 10 15	— — —	1.0 2.0 2.5	— — —	2.25 4.50 6.75	1.0 2.0 2.5	— — —	1.0 2.0 2.5	
(V_O = 0.5 Vdc) "1" Level (V_O = 1.0 Vdc) (V_O = 1.5 Vdc)	I_{IH}	5.0 10 15	4.0 8.0 12.5	— — —	4.0 8.0 12.5	2.75 5.50 8.25	— — —	4.0 8.0 12.5	— — —	Vdc
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)		5.0 5.0 10 15	– 1.2 – 0.25 – 0.62 – 1.8	— — — —	– 1.0 – 0.2 – 0.5 – 1.5	– 1.7 – 0.36 – 0.9 – 3.5	— — — —	– 0.7 – 0.14 – 0.35 – 1.1	— — — —	
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	0.25 0.5 1.0	— — —	0.0005 0.0010 0.0015	0.25 0.5 1.0	— — —	7.5 15 30	µAdc
Total Supply Current (4.) (5.) (Dynamic plus Quiescent, Per Gate C_L = 50 pF)	I_T	5.0 10 15	I_T = (0.3 µA/kHz) f + I_{DD}/N I_T = (0.6 µA/kHz) f + I_{DD}/N I_T = (0.8 µA/kHz) f + I_{DD}/N							µAdc

Serie MC14001UB (unbuffered)

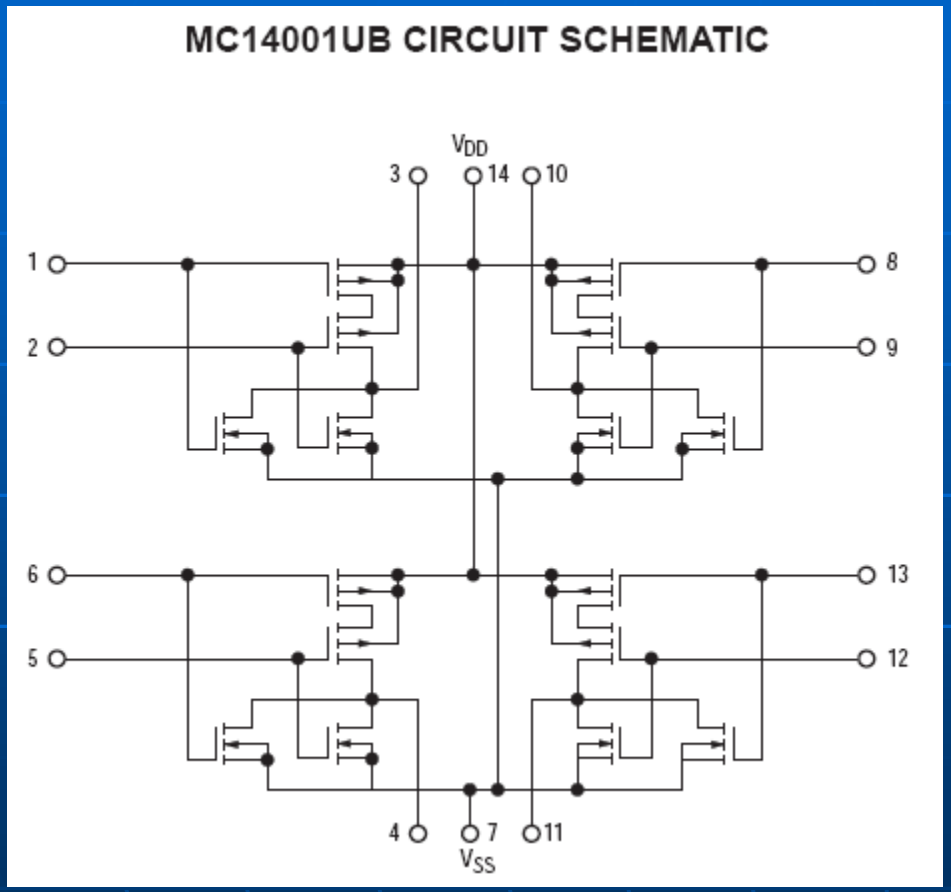
MC14001UB, MC14011UB

SWITCHING CHARACTERISTICS [6.] (C_L = 50 pF, T_A = 25°C)

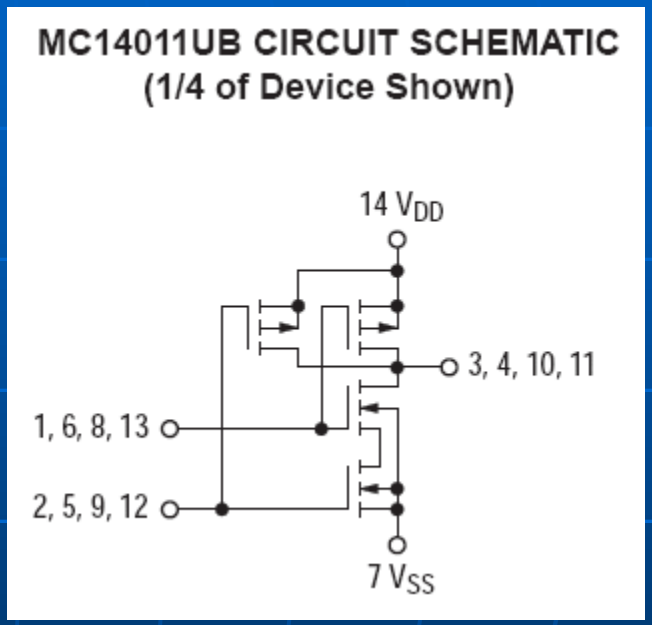
Characteristic	Symbol	V_{DD} Vdc	Min	Typ [7.]	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	—	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	—	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	—	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	—	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 30 ns		5.0	—	90	180	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 22 ns		10	—	50	100	
t_{PLH}, t_{PHL} = (0.50 ns/pF) C_L + 15 ns		15	—	40	80	

Serie MC14001UB (unbuffered)

4 x NOR2



¼ NAND2



Serie MC14001UB (buffered)

alta capacidad de corriente

MC14001B Series

B-Suffix Series CMOS Gates

MC14001B, MC14011B, MC14023B, MC14025B, MC14071B, MC14073B, MC14081B, MC14082B

The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load Over the Rated Temperature Range.
- Double Diode Protection on All Inputs Except: Triple Diode Protection on MC14011B and MC14081B
- Pin–for–Pin Replacements for Corresponding CD4000 Series B Suffix Devices

Familias Lógicas

Serie MC14001B (buffered)

FAMILIA CMOS

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (3.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc)	V_{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
(V_O = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
"1" Level (V_O = 0.5 or 4.5 Vdc)	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Current (V_{OH} = 2.5 Vdc) Source	I_{OH}	5.0	– 3.0	—	– 2.4	– 4.2	—	– 1.7	—	mAdc
(V_{OH} = 4.6 Vdc)		5.0	– 0.64	—	– 0.51	– 0.88	—	– 0.36	—	
(V_{OH} = 9.5 Vdc)		10	– 1.6	—	– 1.3	– 2.25	—	– 0.9	—	
(V_{OH} = 13.5 Vdc)		15	– 4.2	—	– 3.4	– 8.8	—	– 2.4	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	0.25	—	0.0005	0.25	—	7.5	µAdc
		10	—	0.5	—	0.0010	0.5	—	15	
		15	—	1.0	—	0.0015	1.0	—	30	
Total Supply Current (4.) (5.) (Dynamic plus Quiescent, Per Gate, C_L = 50 pF)	I_T	5.0	I_T = (0.3 µA/kHz) f + I_{DD}/N							µAdc
		10	I_T = (0.6 µA/kHz) f + I_{DD}/N							
		15	I_T = (0.9 µA/kHz) f + I_{DD}/N							

MC14001B Series

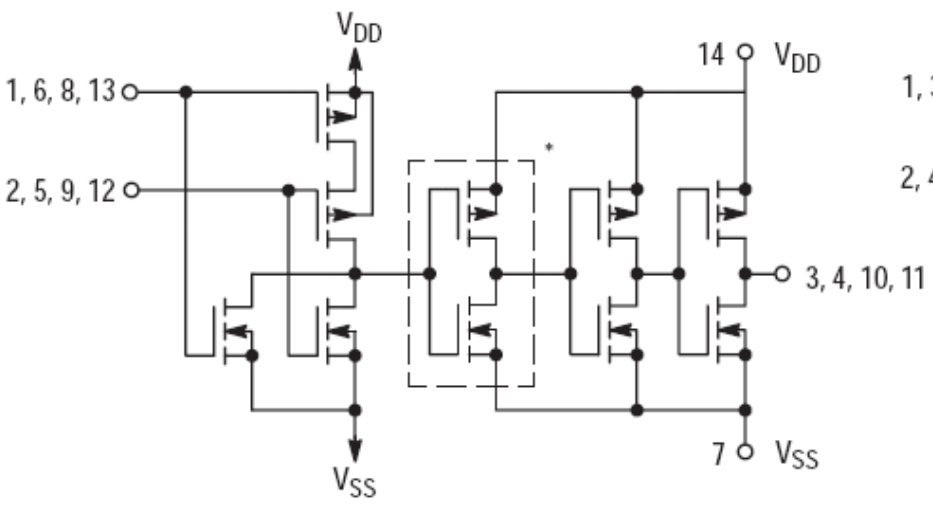
B–SERIES GATE SWITCHING TIMES

SWITCHING CHARACTERISTICS [6.] (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ [7.]	Max	Unit
Output Rise Time, All B–Series Gates	t_{TLH}					ns
t_{TLH} = (1.35 ns/pF) C_L + 33 ns		5.0	—	100	200	
t_{TLH} = (0.60 ns/pF) C_L + 20 ns		10	—	50	100	
t_{TLH} = (0.40 ns/PF) C_L + 20 ns		15	—	40	80	
Output Fall Time, All B–Series Gates	t_{THL}					ns
t_{THL} = (1.35 ns/pF) C_L + 33 ns		5.0	—	100	200	
t_{THL} = (0.60 ns/pF) C_L + 20 ns		10	—	50	100	
t_{THL} = (0.40 ns/pF) C_L + 20 ns		15	—	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
MC14001B, MC14011B only						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 80 ns		5.0	—	125	250	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 32 ns		10	—	50	100	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 27 ns		15	—	40	80	
All Other 2, 3, and 4 Input Gates						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 115 ns		5.0	—	160	300	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 47 ns		10	—	65	130	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 37 ns		15	—	50	100	
8–Input Gates (MC14068B, MC14078B)						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 155 ns		5.0	—	200	350	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 62 ns		10	—	80	150	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 47 ns		15	—	60	110	

Serie MC14001UB (buffered)

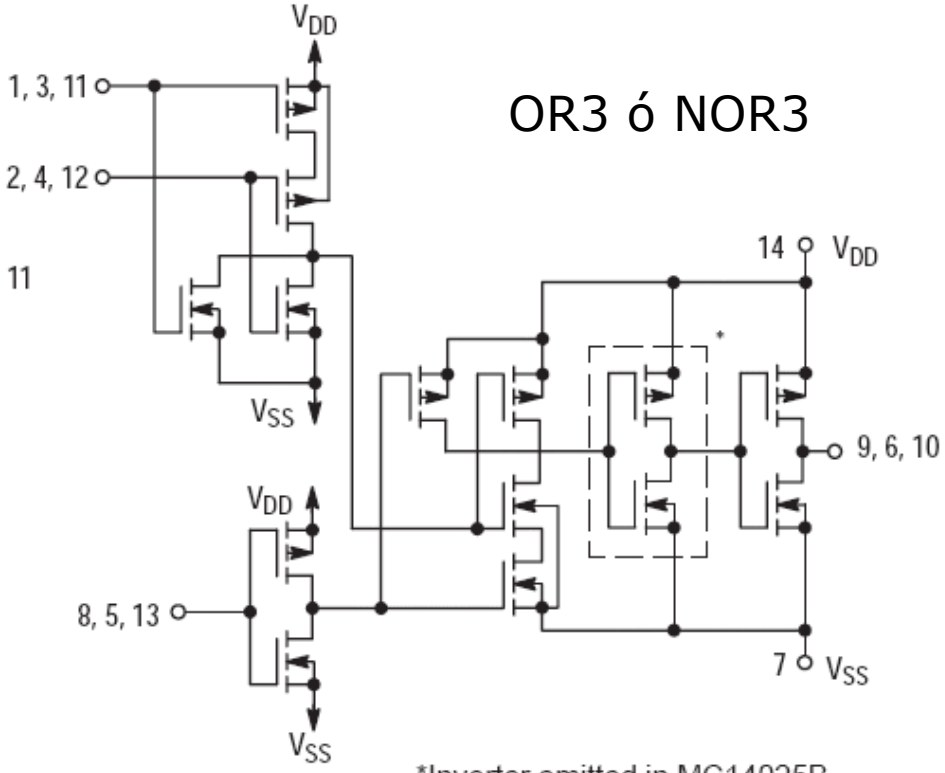
MC14001B, MC14071B
One of Four Gates Shown



*Inverter omitted in MC14001B

OR2 ó NOR2

MC14025B
One of Three Gates Shown

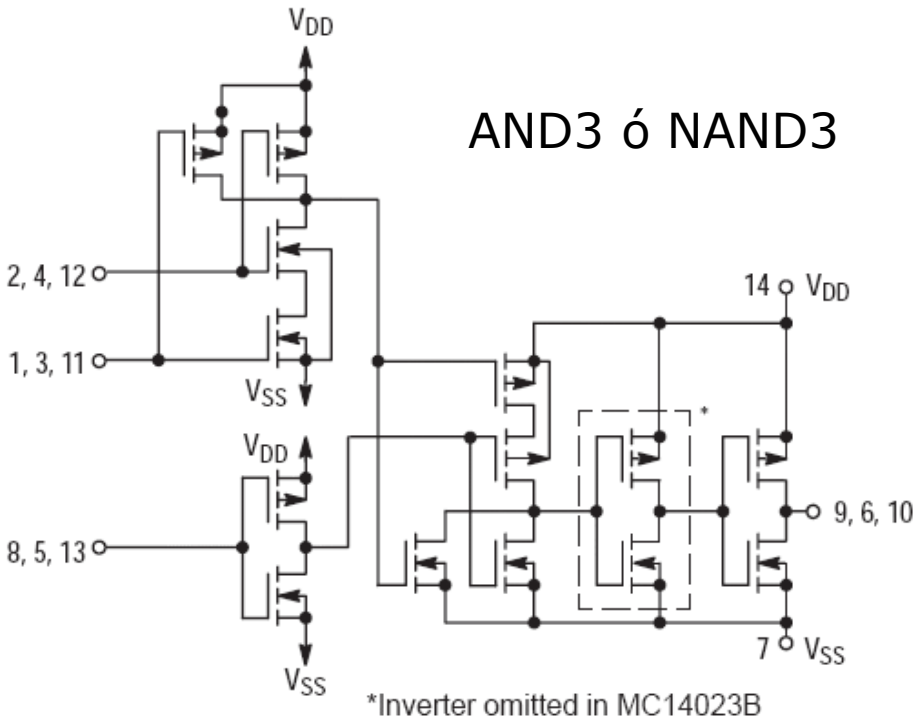


OR3 ó NOR3

*Inverter omitted in MC14025B

Serie MC14001UB (buffered)

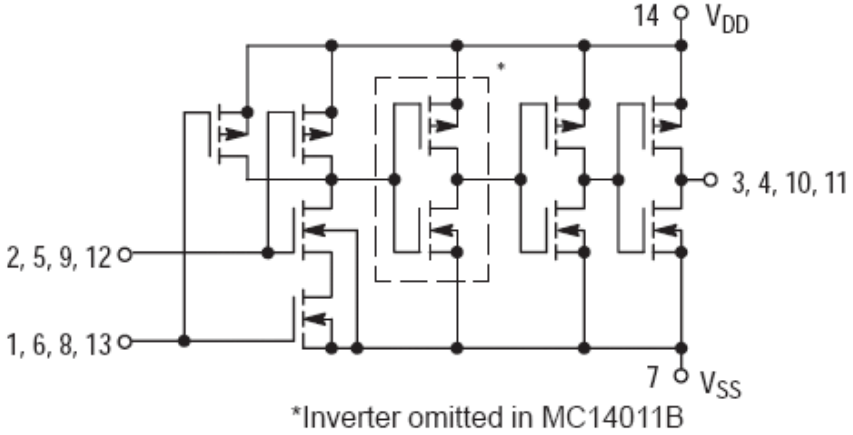
MC14023B, MC14073B
One of Three Gates Shown



*Inverter omitted in MC14023B

AND3 ó NAND3

MC14011B, MC14081B
One of Four Gates Shown



*Inverter omitted in MC14011B

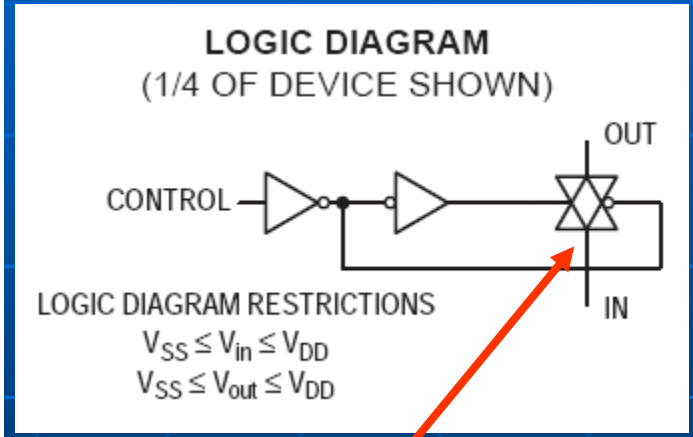
AND2 ó NAND2

MC14016B

Quad Analog Switch/ Quad Multiplexer

The MC14016B quad bilateral switch is constructed with MOS P–channel and N–channel enhancement mode devices in a single monolithic structure. Each MC14016B consists of four independent switches capable of controlling either digital or analog signals. The quad bilateral switch is used in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linearized Transfer Characteristics
- Low Noise — 12 nV/$\sqrt{\text{Cycle}}$, f ≥ 1.0 kHz typical
- Pin–for–Pin Replacements for CD4016B, CD4066B (Note improved transfer characteristic design causes more parasitic coupling capacitance than CD4016)
- For Lower R_{ON}, Use The HC4016 High–Speed CMOS Device or The MC14066B
- This Device Has Inputs and Outputs Which Do Not Have ESD Protection. Antistatic Precautions Must Be Taken.



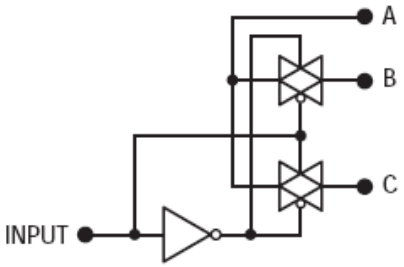
Compuerta pass-gate

MC14007UB

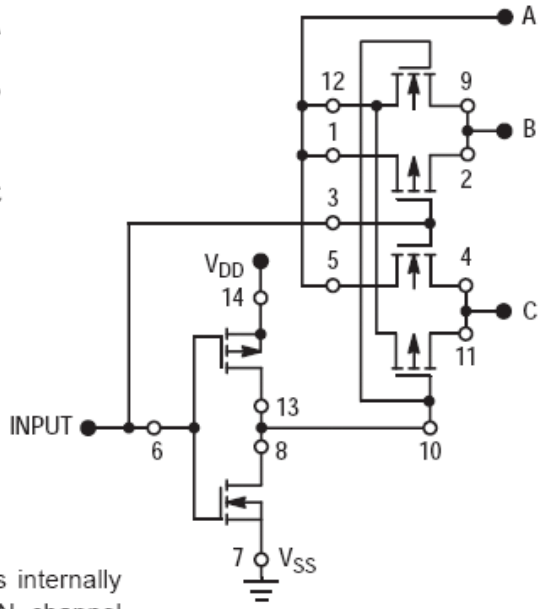
Dual Complementary Pair Plus Inverter

The MC14007UB multi–purpose device consists of three N–channel and three P–channel enhancement mode devices packaged to provide access to each device. These versatile parts are useful in inverter circuits, pulse–shapers, linear amplifiers, high input impedance amplifiers, threshold detectors, transmission gating, and functional gating.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load Over the Rated Temperature Range
- Pin–for–Pin Replacement for CD4007A or CD4007UB
- This device has 2 outputs without ESD Protection. Anti–static precautions must be taken.



INPUT	OUTPUT CONDITION
1	A = C, B = OPEN
0	A = B, C = OPEN



Substrates of P–channel devices internally connected to V_{DD}; substrates of N–channel devices internally connected to V_{SS}.

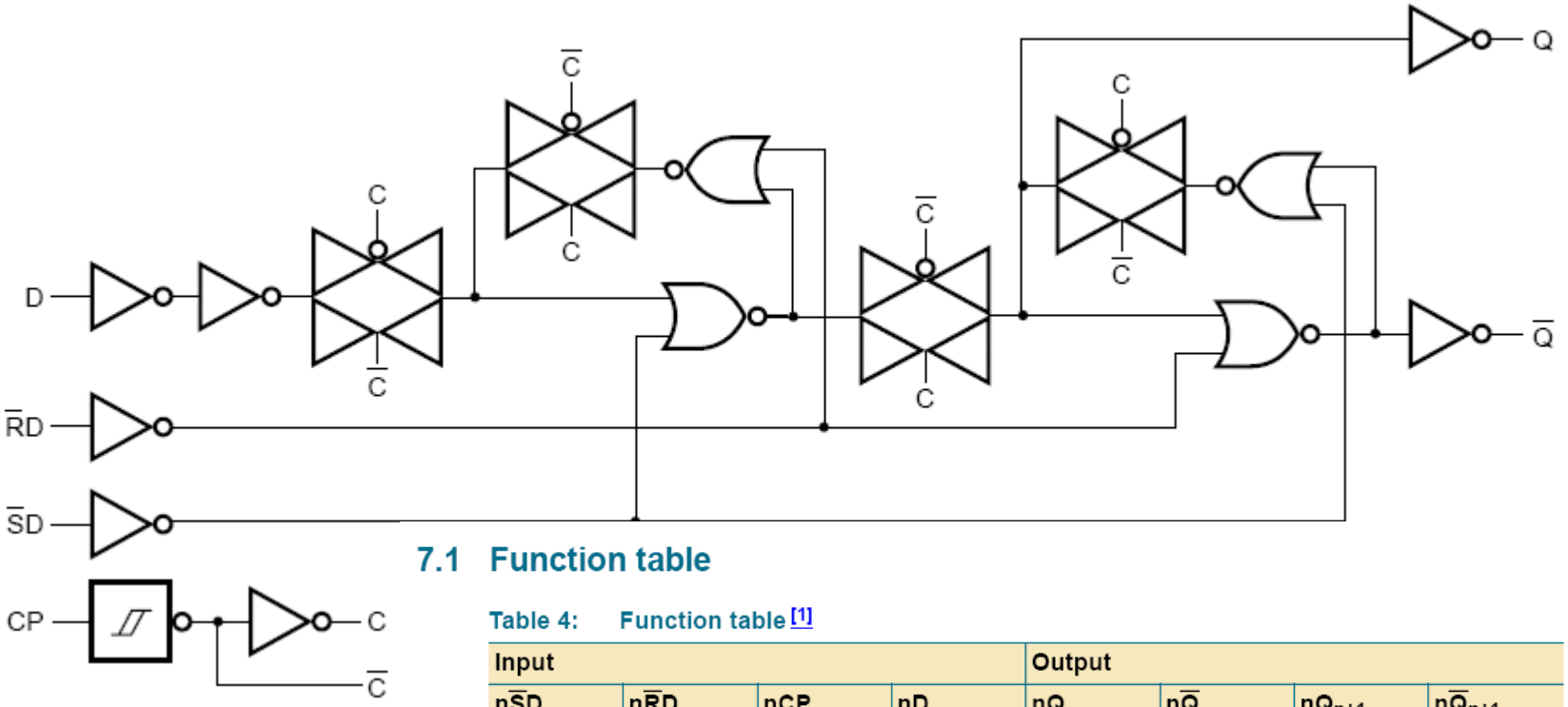
Lógica CMOS

Serie 74XX

Es la mas nueva y actual de CMOS.
Sus mayores ventajas son:
Bajo consumo respecto a las versiones de TTL LPS (Low Power Schottky).
Mayor inmunidad al ruido.
Rango de tensiones de alimentación medio (3 V a 6 V).
Velocidad comparable a TTL LS (depende de las versiones).

En la actualidad tenemos varias versiones:
74HC y 74AC (compatibles con CMOS con rango reducido de Vcc).
74HCT y 74ACT (compatibles con TTL en 5 Volts)
Versiones de baja tensión (74AHC, 74LCX, 74LVX, 74ALCX, etc.)

NOTA: Las denominaciones cambian dependiendo del fabricante.



7.1 Function table

Table 4: Function table [1]

Input				Output			
$n\overline{SD}$	$n\overline{RD}$	nCP	nD	nQ	$n\overline{Q}$	nQ_{n+1}	$n\overline{Q}_{n+1}$
L	H	X	X	H	L	L	H
H	L	X	X	L	H	H	L
L	L	X	X	H	H	-	-
H	H	↑	L	-	-	L	H
H	H	↑	H	-	-	H	L

[1] H = HIGH voltage level;
L = LOW voltage level;
↑ = LOW-to-HIGH transition;
Q_{n+1} = state after the next LOW-to-HIGH CP transition;
X = don't care.

FLIP-FLOP TIPO "D" sensible a flanco ascendente con entradas de set y reset

Familias Lógicas

74AHC74/AHCT74

FAMILIA CMOS

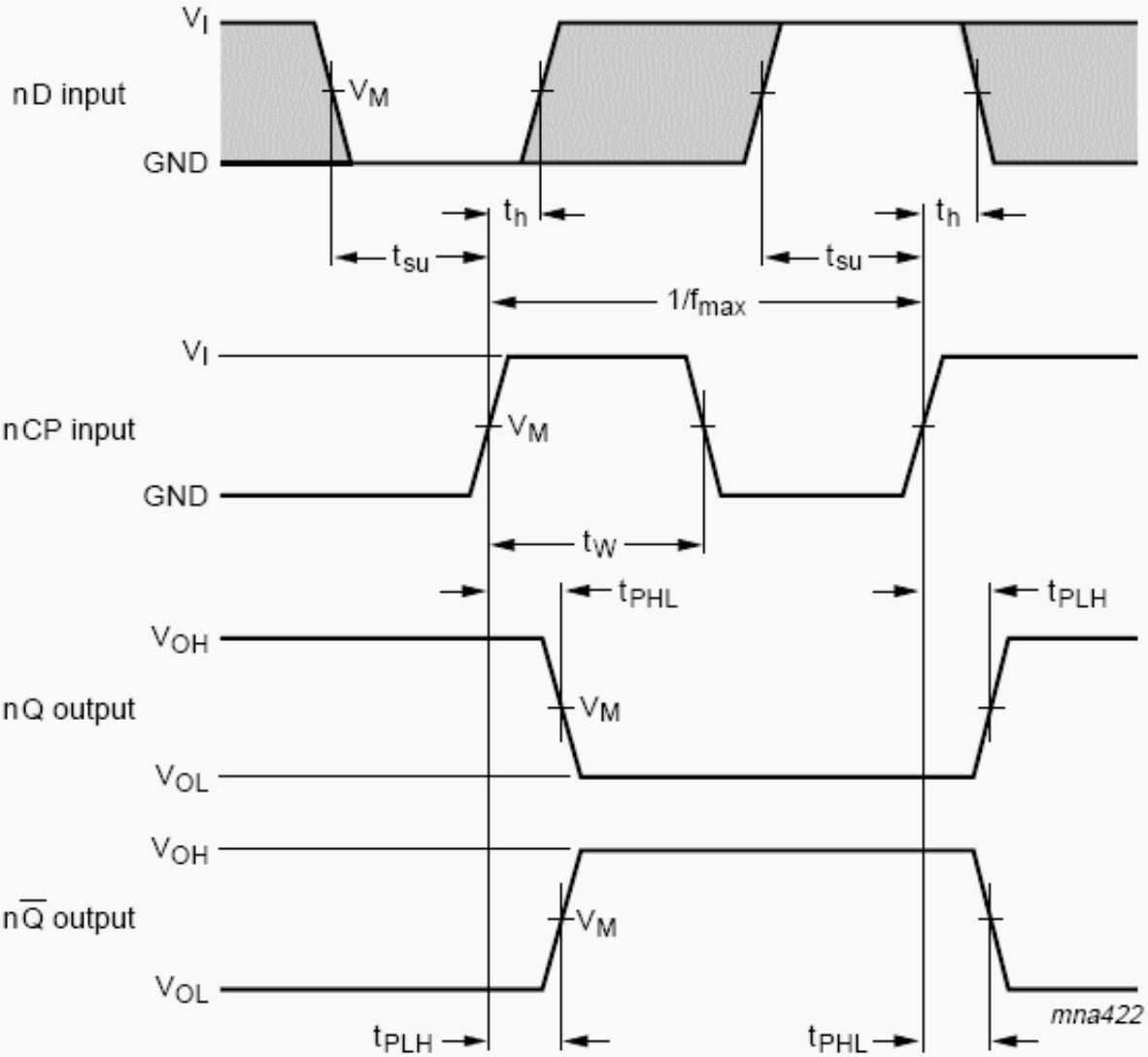
Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C [1]						
t_{PHL}, t_{PLH}	propagation delay					
	nCP to nQ, n$\overline{Q}$	V_{CC} = 3.0 V to 3.6 V; see Figure 7				
		C_L = 15 pF	-	5.2	11.9	ns
		C_L = 50 pF	-	7.4	15.4	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 7				
		C_L = 15 pF	-	3.7	7.3	ns
		C_L = 50 pF	-	5.2	9.3	ns
	n$\overline{SD}$, n$\overline{RD}$ to nQ, n$\overline{Q}$	V_{CC} = 3.0 V to 3.6 V; see Figure 8				
		C_L = 15 pF	-	5.4	12.3	ns
		C_L = 50 pF	-	7.7	15.8	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 8				
		C_L = 15 pF	-	3.7	7.7	ns
		C_L = 50 pF	-	5.3	9.7	ns
f_{max}	maximum clock pulse frequency	V_{CC} = 3.0 V to 3.6 V; see Figure 7				
		C_L = 15 pF	80	125	-	MHz
		C_L = 50 pF	50	75	-	MHz
		V_{CC} = 4.5 V to 5.5 V; see Figure 7				
		C_L = 15 pF	130	170	-	MHz
		C_L = 50 pF	90	115	-	MHz
t_W	pulse width					
	clock pulse HIGH or LOW	C_L = 50 pF; see Figure 7				
		V_{CC} = 3.0 V to 3.6 V	6.0	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	5.0	-	-	ns
	set or reset pulse LOW	C_L = 50 pF; see Figure 8				
		V_{CC} = 3.0 V to 3.6 V	6.0	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	5.0	-	-	ns

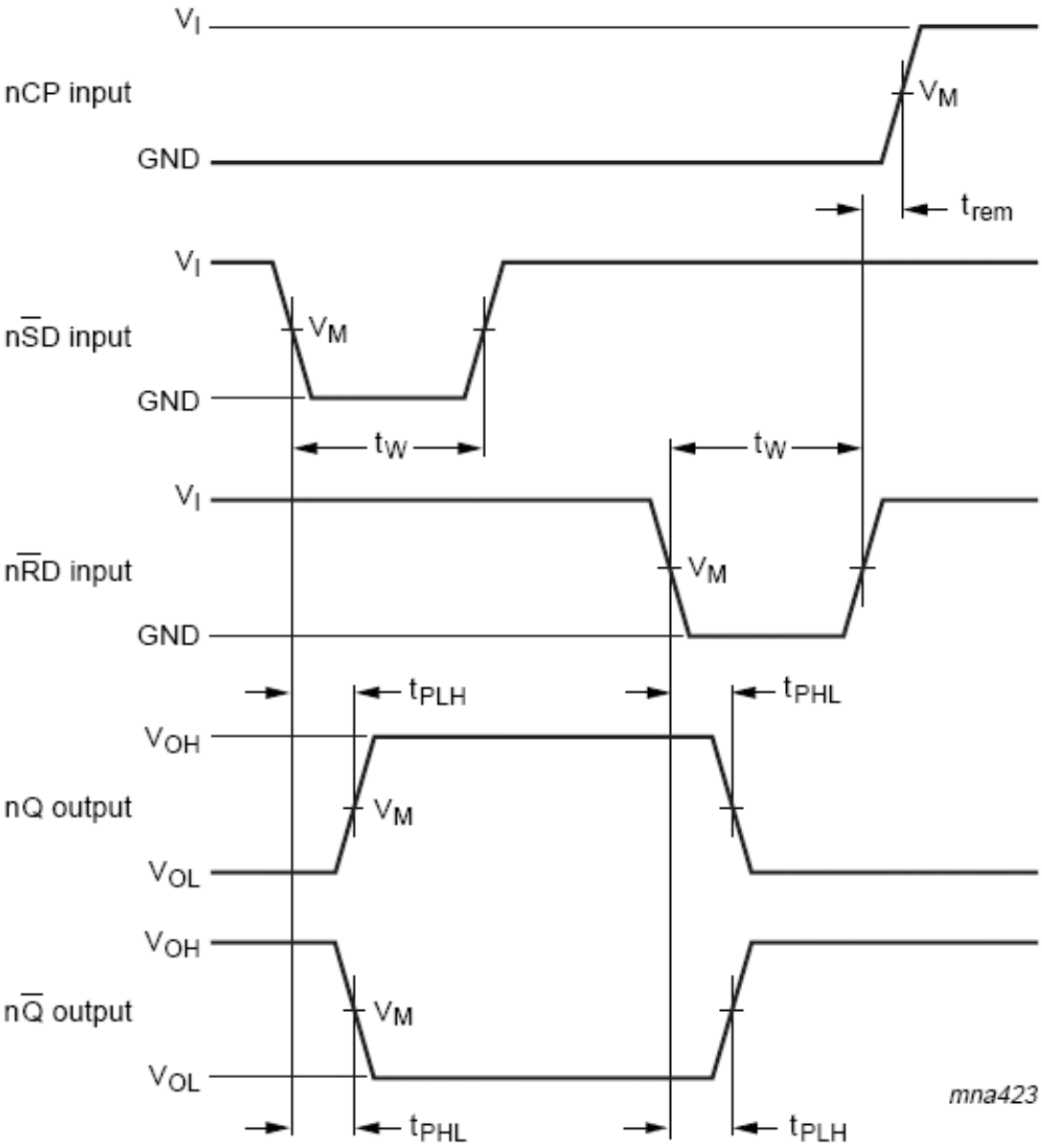
Hay anchos mínimos de pulso que se deben respetar

Familias Lógicas

74AHC74/AHCT74

Diagramas de tiempo: Salidas vs. reloj

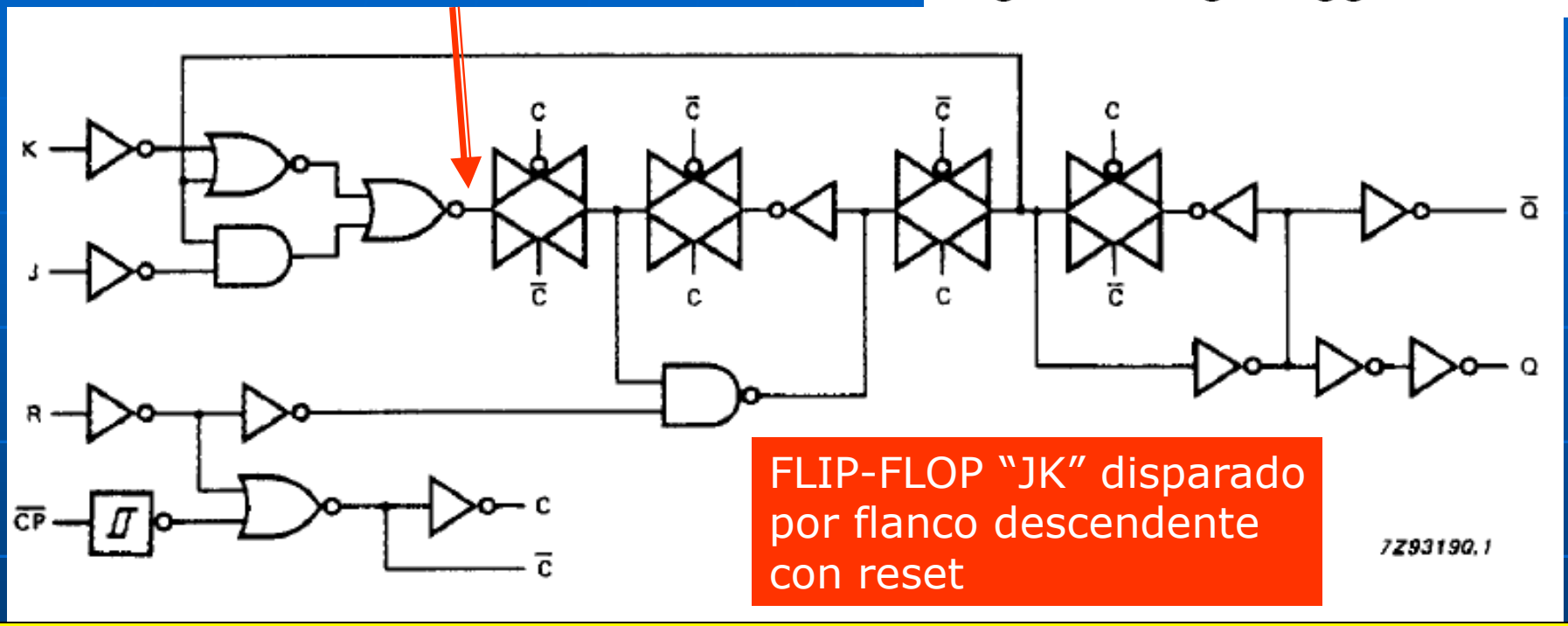




Diagramas de tiempo: Salidas vs. entradas asincrónicas

$$P = \overline{(\overline{J} \cdot \overline{Q}) + (\overline{\overline{K} + \overline{Q}})}$$

74HC/HCT107
Dual JK flip-flop with reset; negative-edge trigger



FLIP-FLOP "JK" disparado por flanco descendente con reset

Si $J = \overline{K}$ => $P = \overline{(\overline{J} \cdot \overline{Q}) + (\overline{J} + \overline{Q})} = (J + Q) \cdot (J + \overline{Q}) = J$ **(Funciona como "D")**

Si J = K => $P = \overline{(\overline{J} \cdot \overline{Q}) + (\overline{J} + \overline{Q})} = (J + Q) \cdot (\overline{J} + \overline{Q}) = J \oplus Q$ **(Funciona como "T")**

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $n\overline{CP}$ to nQ		52 19 15	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $n\overline{CP}$ to $n\overline{Q}$		52 19 15	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $n\overline{R}$ to nQ, $n\overline{Q}$		52 19 15	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig.7
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6
t_W	clock pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t_W	reset pulse width LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t_{rem}	removal time $n\overline{R}$ to $n\overline{CP}$	60 12 10	19 7 6		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.7
t_{su}	set-up time nJ, nK to $n\overline{CP}$	100 20 17	22 8 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig.6
t_h	hold time nJ, nK to $n\overline{CP}$	3 3 3	−6 −2 −2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig.6
f_{max}	maximum clock pulse frequency	6.0 30 35	23 70 85		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.6

FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$n\overline{R}$	$n\overline{CP}$	J	K	Q	$\overline{Q}$
asynchronous reset	L	X	X	X	L	H
toggle	H	↓	h	h	$\overline{q}$	q
load “0” (reset)	H	↓	l	h	L	H
load “1” (set)	H	↓	h	l	H	L
hold “no change”	H	↓	l	l	q	$\overline{q}$

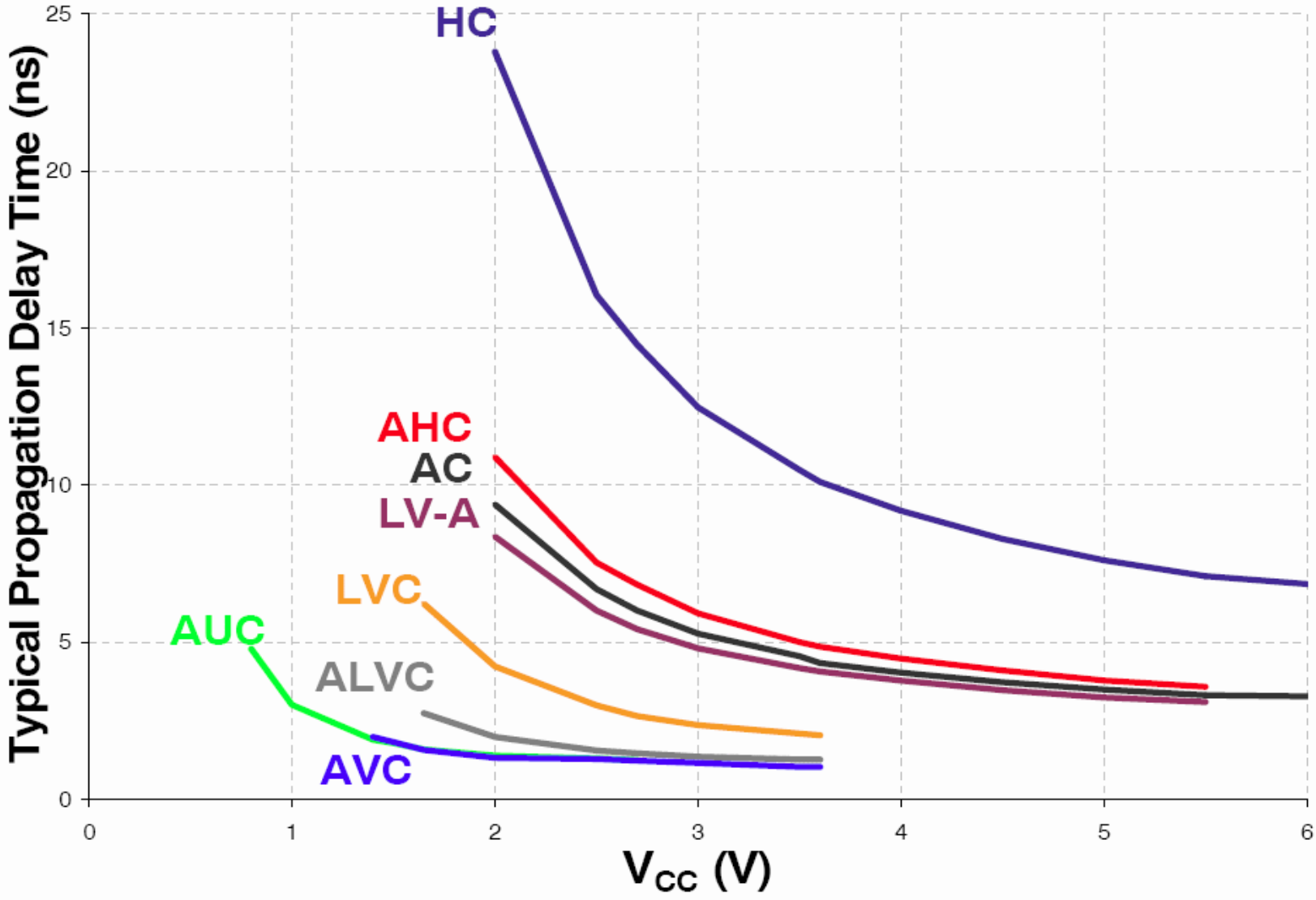
Note

1. H = HIGH voltage level
   h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition
   L = LOW voltage level
   l = LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition
   q = lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW CP transition
   X = don’t care
   ↓ = HIGH-to-LOW CP transition

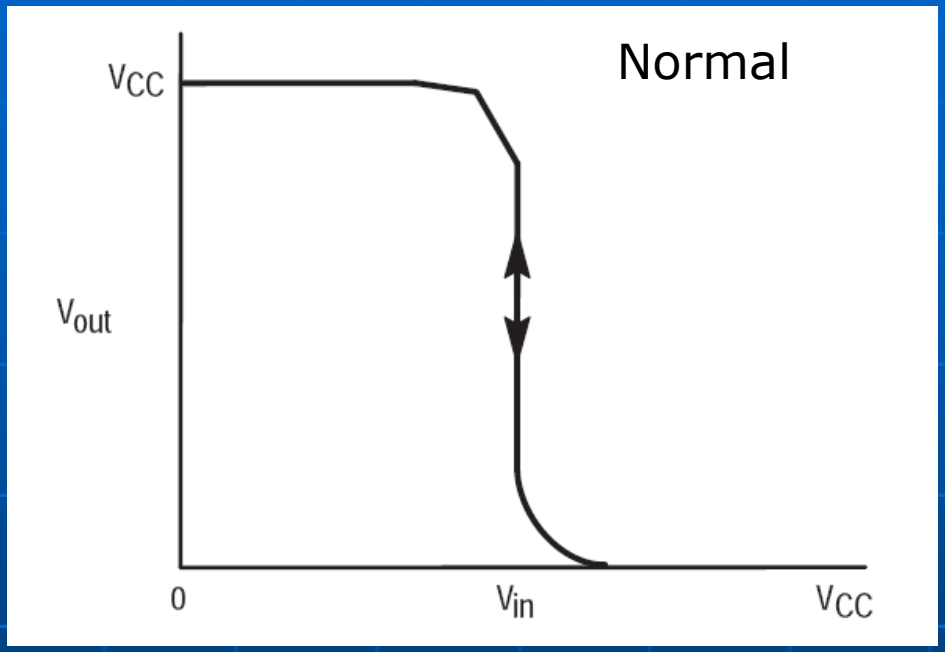
Familias Lógicas

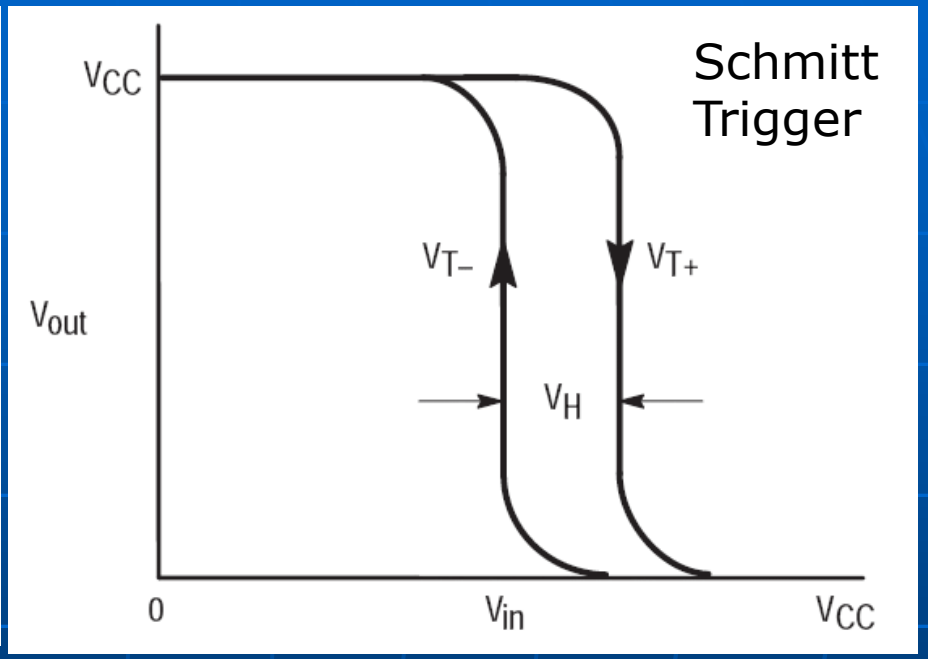
FAMILIA CMOS

Comparación de velocidad vs. tesnsión de alimentación (Vdd)



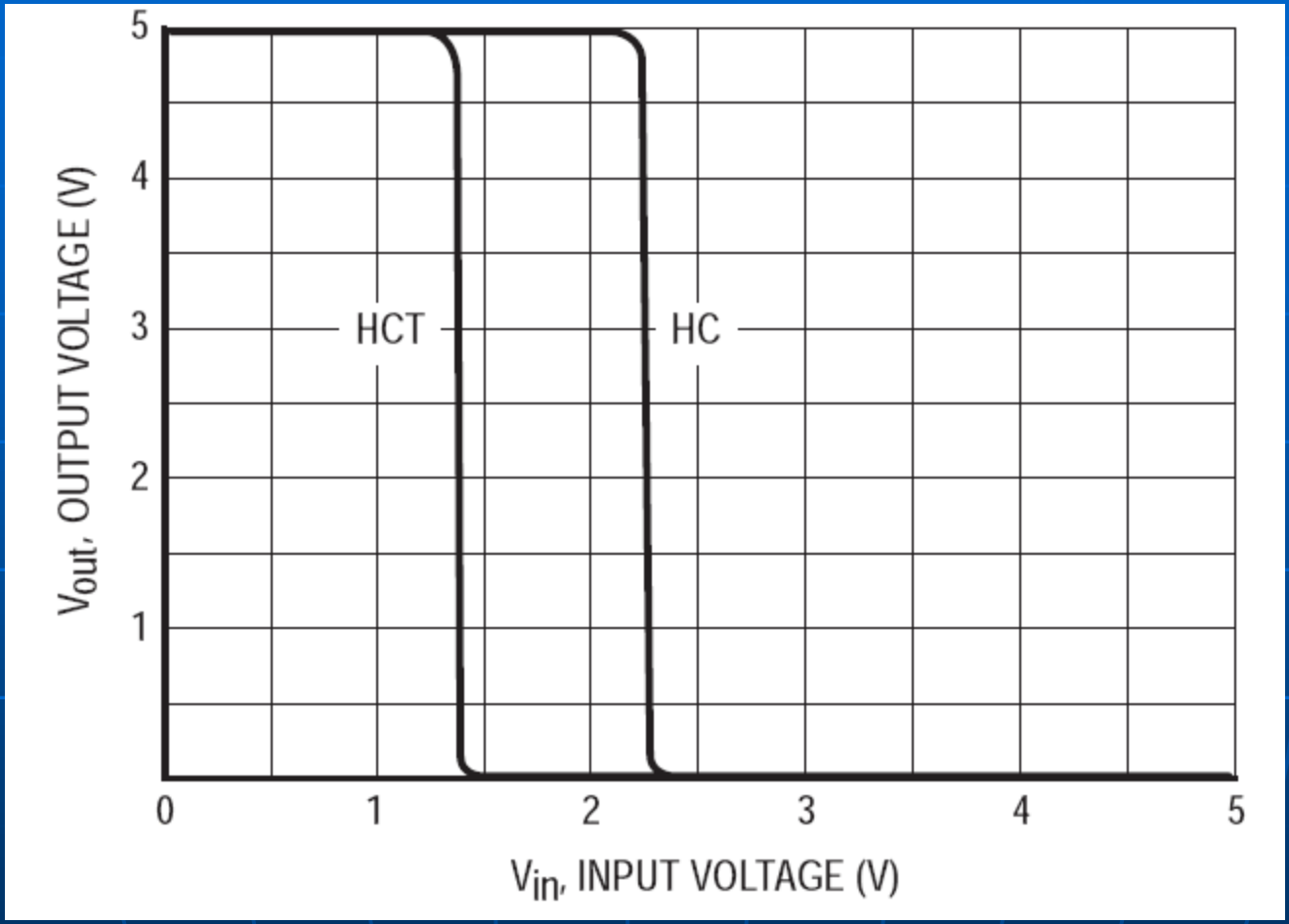
Función de transferencia compuertas Schmitt-Trigger





Permite mayor inmunidad al ruido al existir una histéresis (V_H).

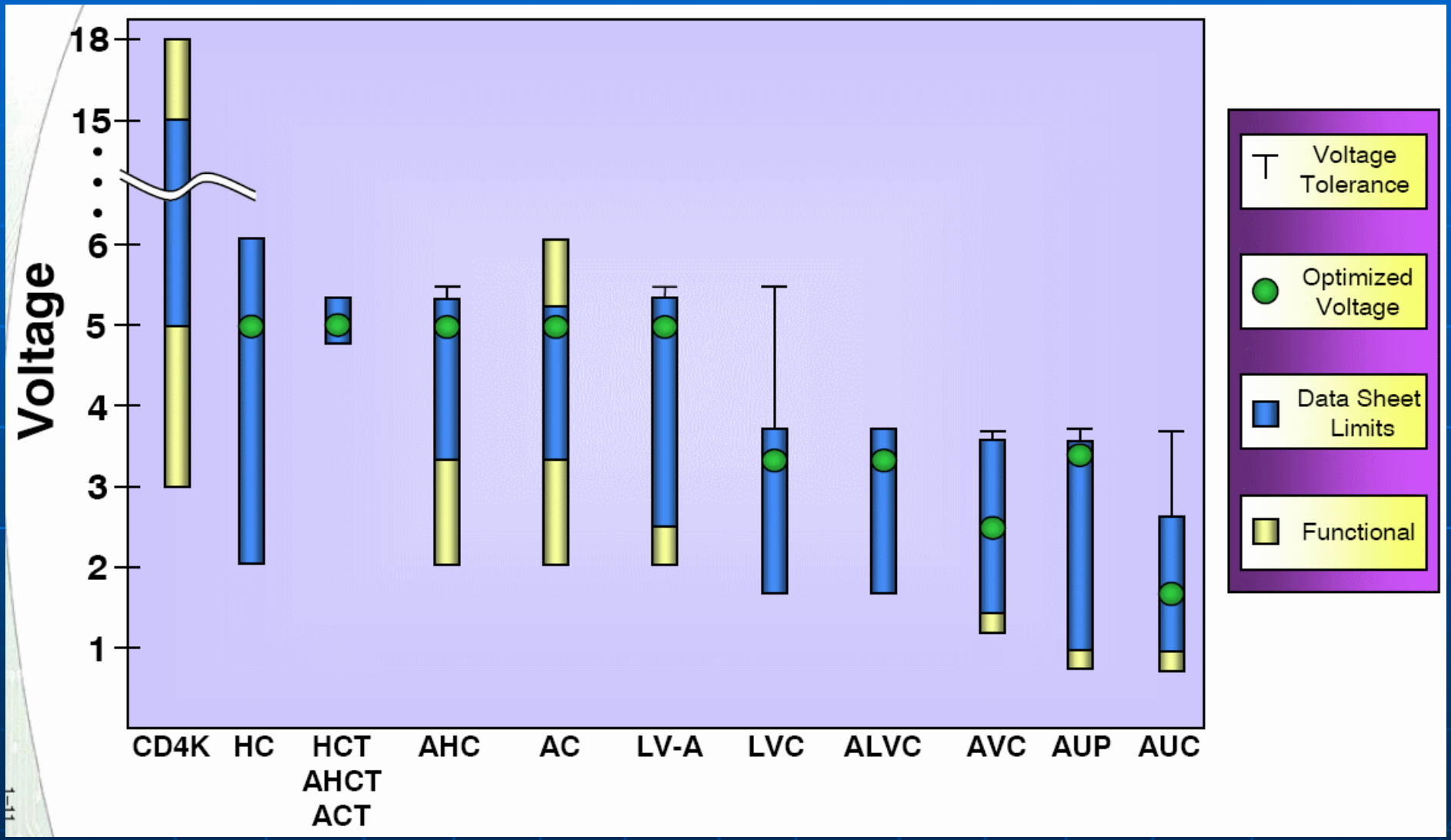
Función de transferencia series HC y HCT



HCT es una versión CMOS que compatibiliza los niveles de tensiones de entrada como TTL, lo que permite conectar a una salida TTL una entrada CMOS 74HCT de igual tensión de alimentación.

Familias Lógicas

Rangos de Vdd en subfamilias CMOS



Familias Lógicas

Comparación de tecnologías en 3,3 V

3.3-V Logic

Technology	V_{CC} (V)	V_{CC} Range	t_{pd} max (ns)	I/O Tolerance (V)	Input Compatibility	Output Compatibility	Port	I_{OH} (max) (mA)	I_{OL} (max) (mA)	Static Current I_{CC} (µA)	Isolation Level*
Bipolar											
ALB	3.3	3.0 to 3.6	2.0	V_{CC} + 0.5	Custom	Custom	Both	Ð25	25	800	0
BiCMOS											
ALVT	3.3	2.3 to 3.6	3.5	5	LVTTL/TTL	LVTTL	Both	Ð8	24	4.5 mA	2
LVT	3.3	2.7 to 3.6	3.5	5	LVTTL/TTL	LVTTL	Both	Ð32	64	190	2
VME	3.3	3.15 to 3.45	14.5	5	LVTTL/TTL	LVTTL/TTL	A	Ð24	24	30 mA	3
							B	Ð48	64		
CMOS											
ALVC	3.3	1.65 to 3.6	3.0	V_{CC}	LVTTL/TTL	LVCMOS	Both	Ð24	24	20	0
ALVCF	3.3	2.3 to 3.6	3.5	V_{CC}	LVTTL/TTL	LVCMOS	Both	Ð12	12	40	0
AUP1G/2G/3G	3.3	0.8 to 3.6	4.0	3.6	LVCMOS	LVCMOS	Both	Ð4	4	0.9	1
CBTLV	3.3	2.3 to 3.6	0.25	3.6	LVCMOS	LVCMOS	Both	N/A	N/A	10	1
CBTLV1G	3.3	2.3 to 3.6	0.25	3.6	LVCMOS	LVCMOS	Both	N/A	N/A	10	1
CB3Q	3.3	2.3 to 3.6	0.2	5	LVTTL/TTL	LVTTL/TTL	Both	N/A	N/A	0.7 mA	1
CB3T	3.3	2.3 to 3.6	0.2	5	TTL	TTL	Both	N/A	N/A	40	1
GTL	3.3	3.15 to 3.45	6.5	5	LVTTL/TTL	GTL	A	Ð24	24	80 mA	1
					GTL	LVTTL/TTL	B	N/A	50		
GTLP	3.3	3.15 to 3.45	7.7	5	LVTTL/TTL	GTLP	A	Ð24	24	40 mA	3
				4.6	GTLP	LVTTL/TTL	B	N/A	100		
HSTL	3.3	3.15 to 3.45	5.0	3.3	HSTL	LVTTL	D	N/A	N/A	50 mA	0
				N/A	N/A		Q	Ð24	24		
LV-A	3.3	2.0 to 5.5	14.0	5	LVCMOS	LVTTL	Both	Ð8	8	20	1
LVC	3.3	1.65 to 3.6	4.0	5.5	LVTTL/TTL	LVCMOS	Both	Ð24	24	10	1
LVC1G/2G/3G	3.3	1.65 to 5.5	3.5	5.5	LVTTL	LVTTL	Both	Ð24	24	10	1
LVCZ	3.3	2.7 to 3.6	4.0	5.5	LVTTL/TTL	LVCMOS	Both	Ð24	24	60	2
SSTL	3.3	2.3 to 3.6	3.7	3.3	SSTL_3	SSTL_3	D/A	N/A	N/A	90 mA	0
				N/A	N/A		Q/Y	Ð20	20		

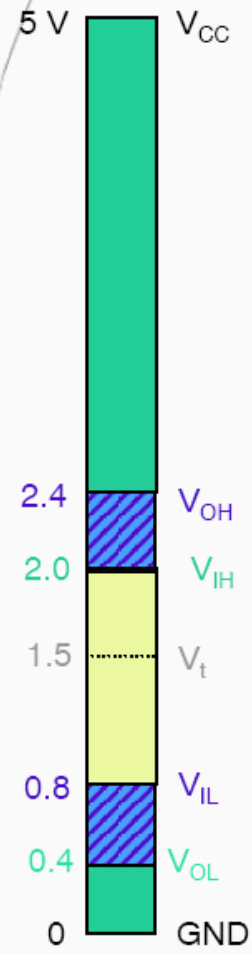
Familias Lógicas

Comparación de tecnologías en 2,5 V y 1,8 V

	Technology	V_{CC} (V)	V_{CC} Range	t_{pd} max (ns)	I/O Tolerance (V)	Input Compatibility	Output Compatibility	Port	I_{OH} (max) (mA)	I_{OL} (max) (mA)	Static Current I_{CC} (µA)	Isolation Level*
2.5-V Logic	CMOS											
	AVC	2.5	1.4 to 3.6	2.0	3.6	LVCMOS	LVCMOS	Both	Ð8	8	20	1
	SSTV	2.5	2.3 to 2.7	2.8	3.3	SSTL_2	SSTL_2	D	N/A	N/A	56 mA	0
					N/A	N/A	Class 2	Q	Ð16	16		
	SSTVF	2.5	2.3 to 2.7	2.6	3.3	SSTL_2	SSTL_2	D	N/A	N/A	56 mA	0
					N/A	N/A	Class 1	Q	Ð16	16		
1.8-V Logic	CMOS											
	AUC	1.8	0.8 to 2.7	2.0	3.6	LVCMOS	LVCMOS	Both	Ð8	8	10	1
	AUC1G/2G/3G	1.8	0.8 to 2.7	2.0	3.6	LVCMOS	LVCMOS	Both	Ð8	8	10	1
	SSTU	1.8	1.7 to 1.9	2.5	2.3	SSTL_18	SSTL_18	D	N/A	N/A	50 mA	0
					N/A	N/A		Q	Ð8	8		

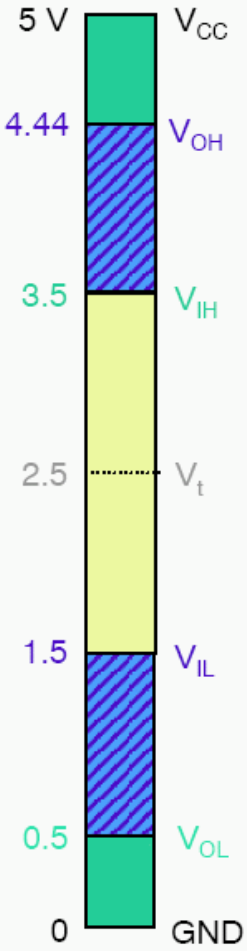
Familias Lógicas

Rango de tensiones de operación



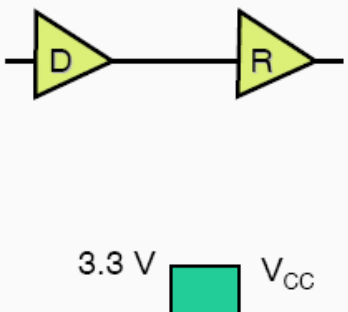
5-V TTL

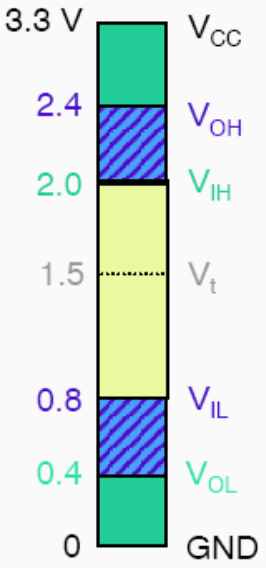
Standard TTL: ABT, AHCT, HCT, ACT, Bipolar



5-V CMOS

Rail-to-Rail 5 V HC, AHC, AC, LV-A



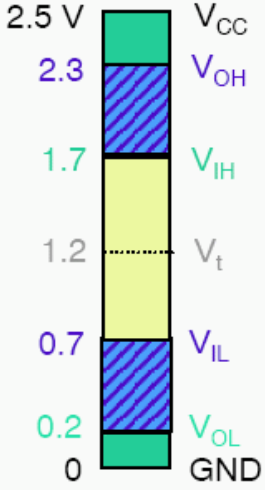


3.3-V LVTTL

LVT, LVC, ALVC AUP, LV-A, ALVT

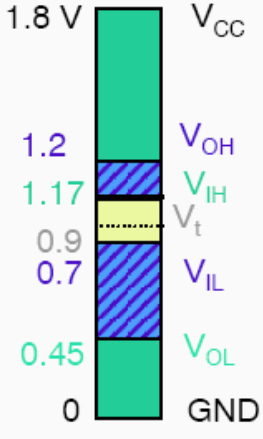
D \ R	5TTL	5CMOS	3LVTTL	2.5CMOS	1.8CMOS
5TTL	Yes	No	Yes *	Yes*	Yes*
5 CMOS	Yes	Yes	Yes*	Yes*	Yes*
3 LVTTL	Yes	No	Yes	Yes*	Yes*
2.5 CMOS	Yes	No	Yes	Yes	Yes*
1.8 CMOS	No	No	No	No	Yes

* Requires V_{IH} Tolerance



2.5-V CMOS

AUC, AUP, AVC, ALVC, LVC, ALVT



1.8-V CMOS

AUC, AUP, AVC, ALVC, LVC

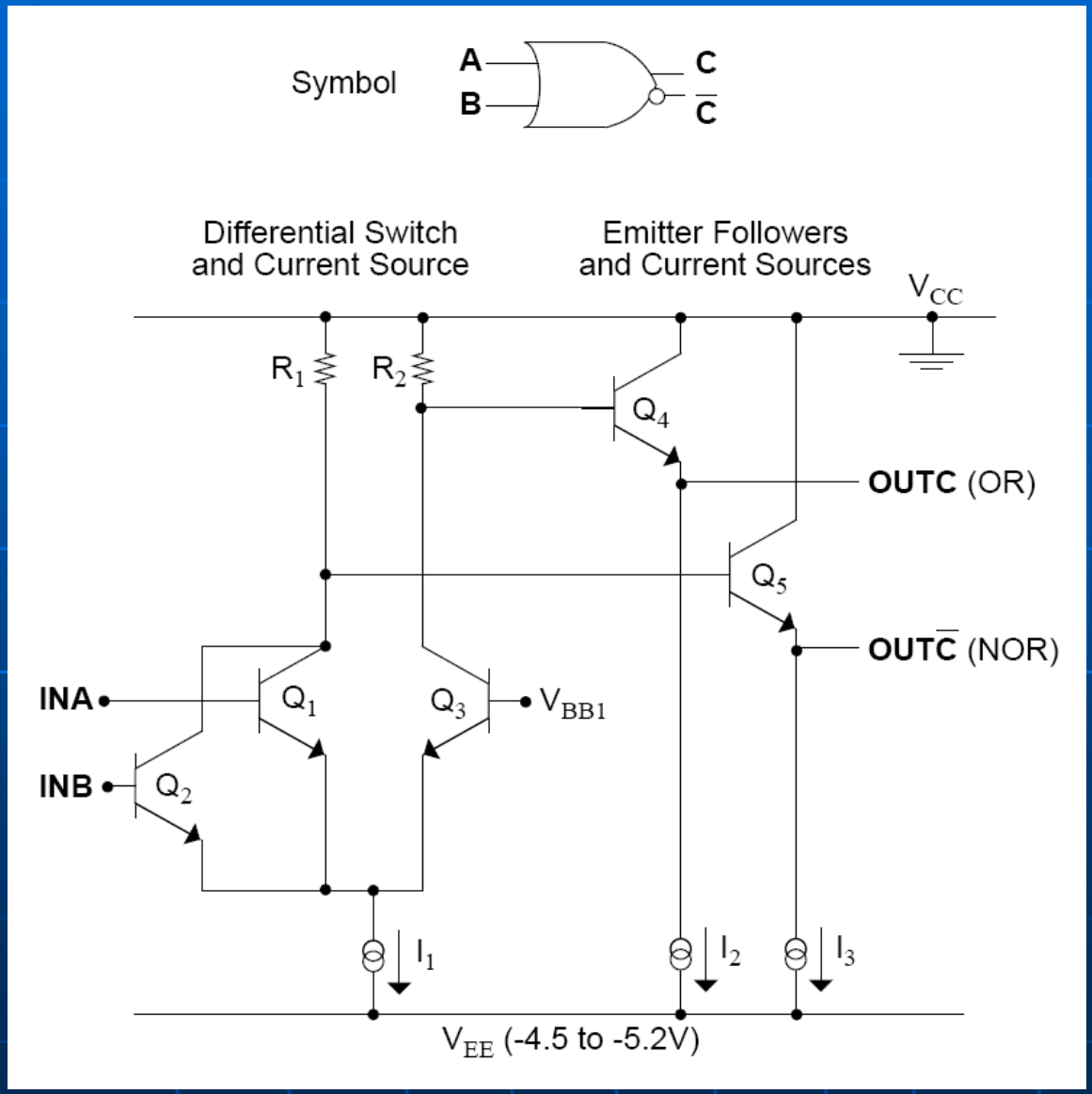
Tecnología ECL

Tecnología ECL
Ventaja: Velocidad y márgen de ruido
Desventaja: Fuente negativa de tensión (-5.2V) y elevado Consumo.
Tecnología PECL
Ventaja: Fuente positiva (desplazada a +5V).
Mantiene características de ECL (swing de 800mV)
Tecnología LVPECL
Ventaja: Fuente de +3.3V. Reduce consumo de potencia.

Familias Lógicas

Tecnología ECL

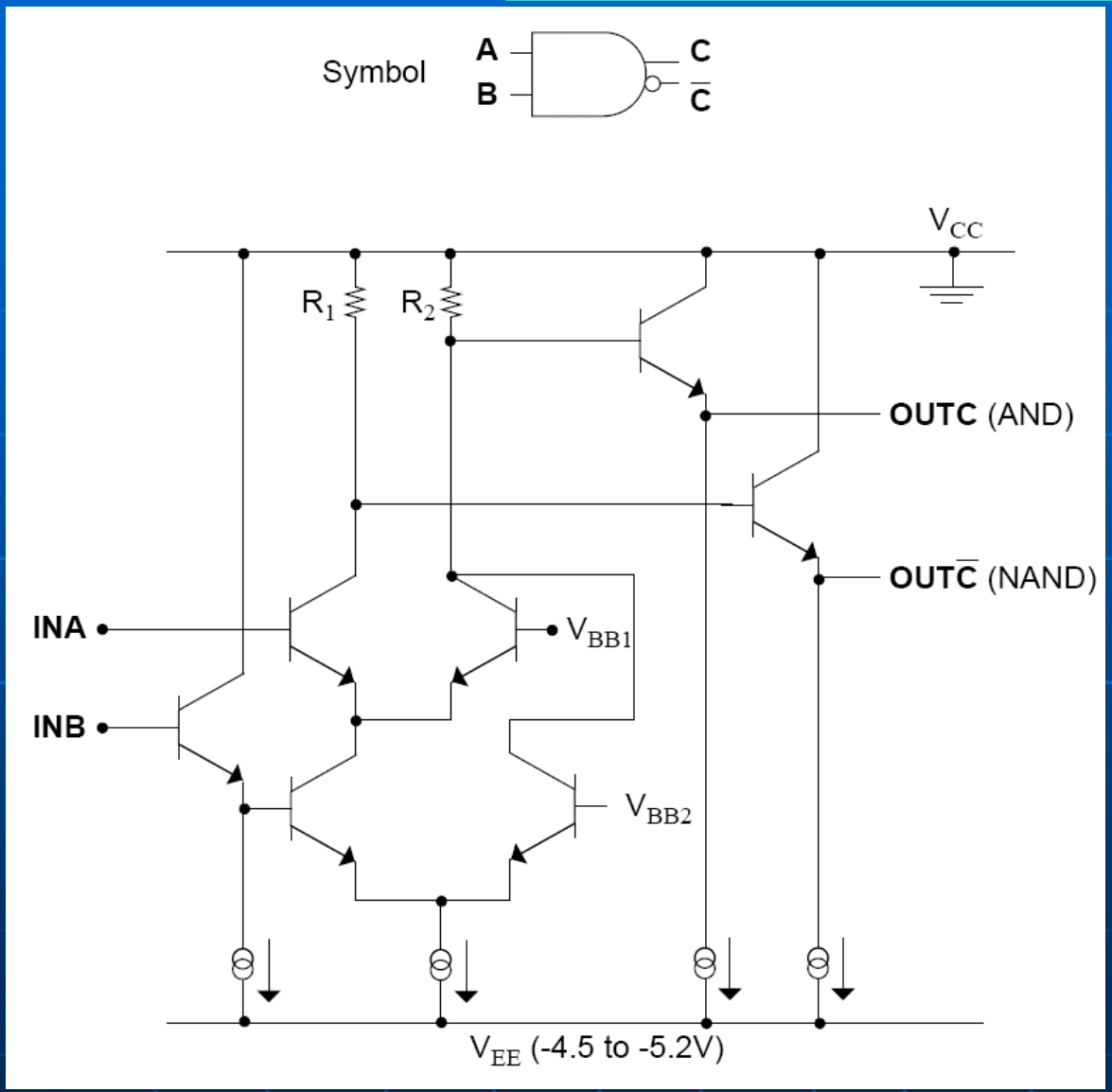
Compuerta OR-NOR en ECL



Familias Lógicas

Tecnología ECL

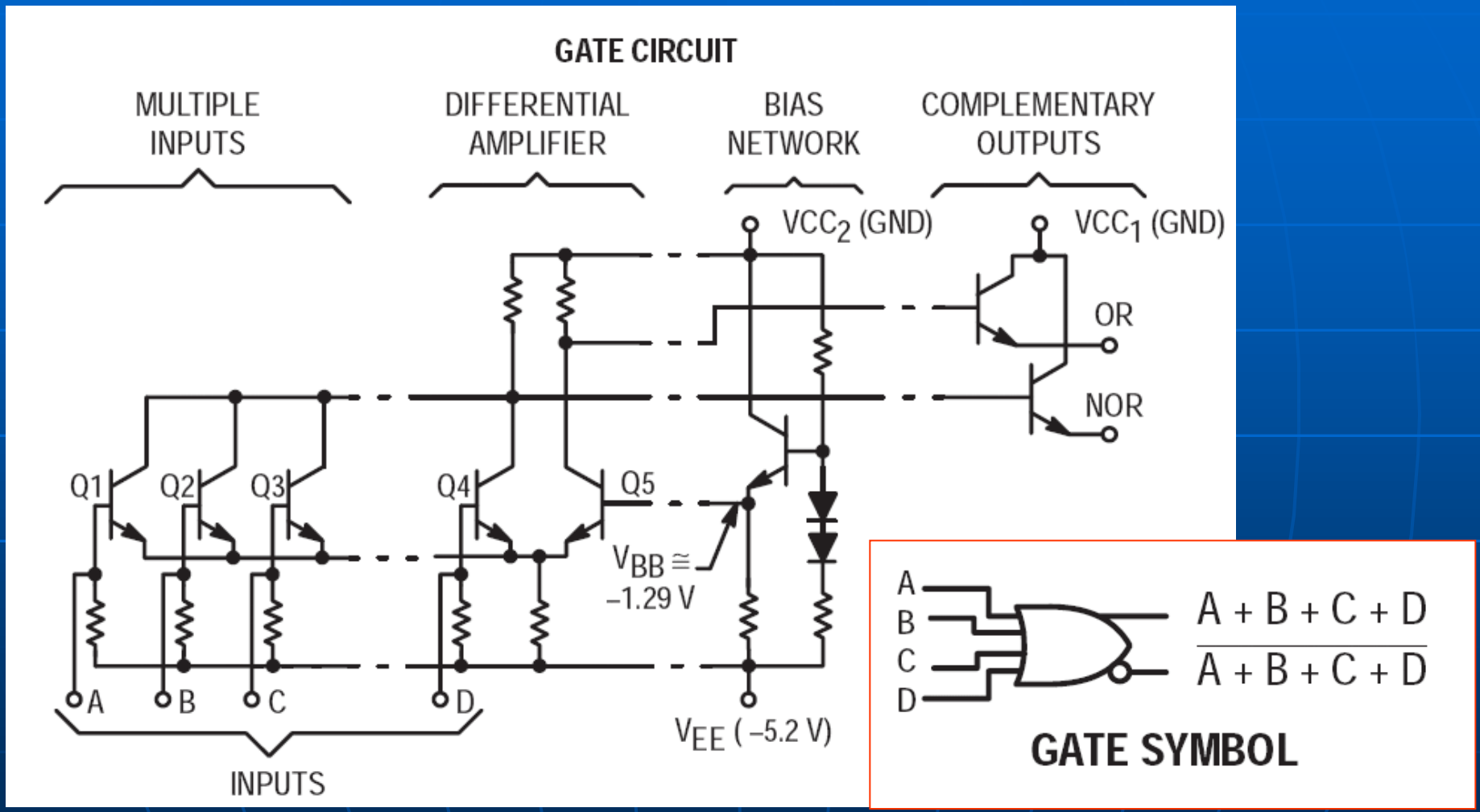
Compuerta AND-NAND en ECL



Familias Lógicas

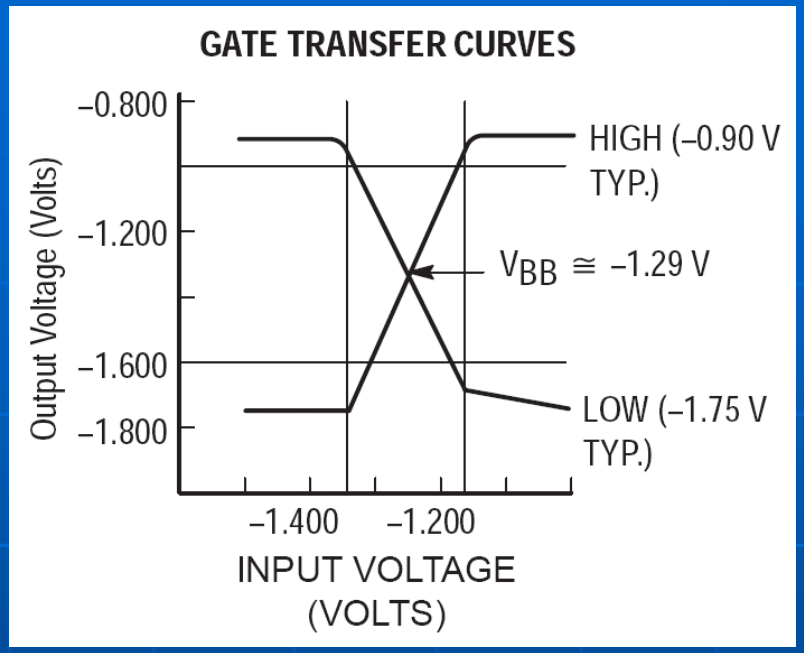
FAMILIA ECL

Ejemplo de compuerta OR-NOR de 4 entradas ECL serie 10K

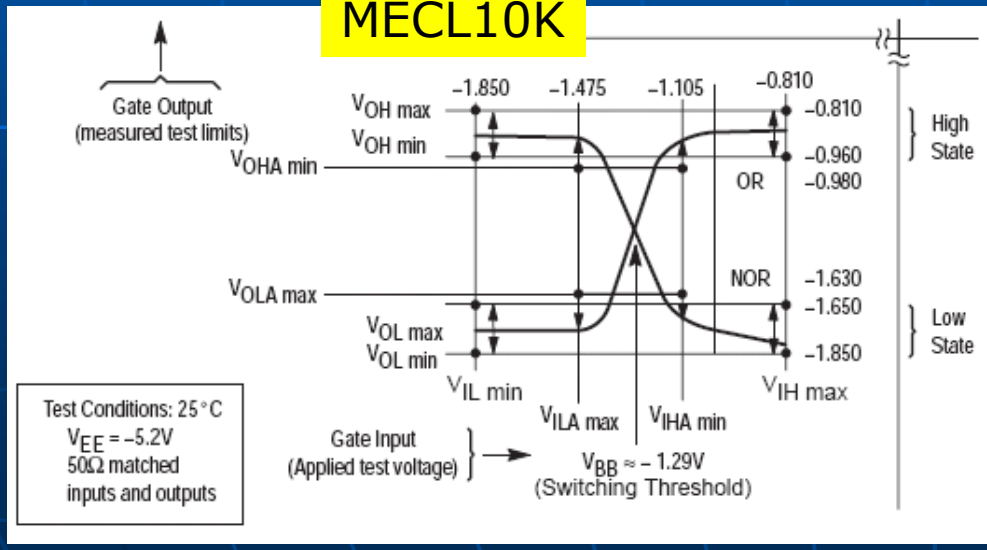


Familias Lógicas

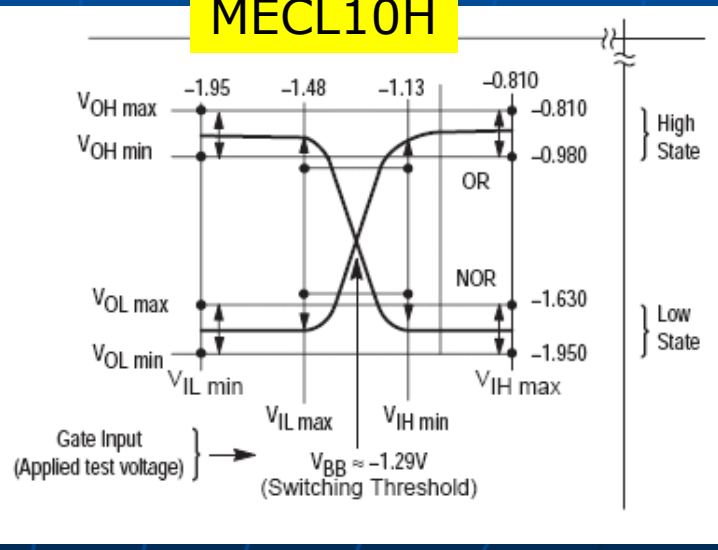
Función de transferencia general de ECL



MECL10K



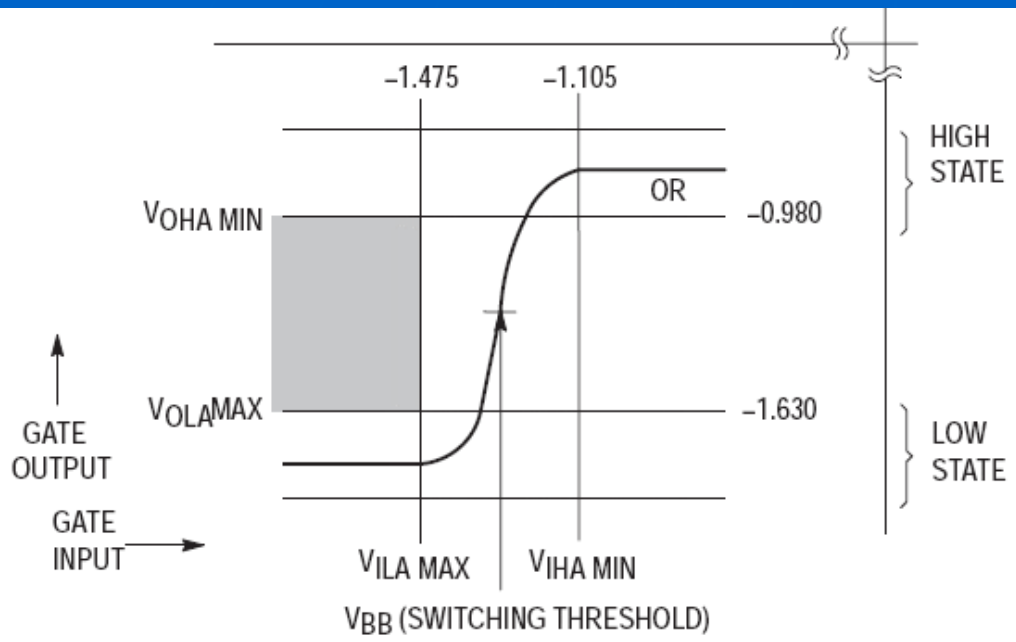
MECL10H



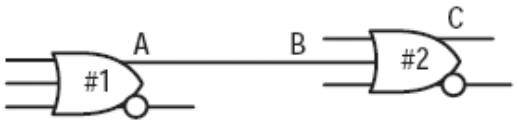
Familias Lógicas

FAMILIA ECL

Márgenes de ruido para MECL10K/10H



Specification Points for Determining Noise Margin



ΔV = High Noise Margin { $V_{OHA\ MIN}$ *, $V_{IHA\ MIN}$ * }

ΔV = Low Noise Margin { $V_{ILA\ MAX}$ *, $V_{OLA\ MAX}$ * }

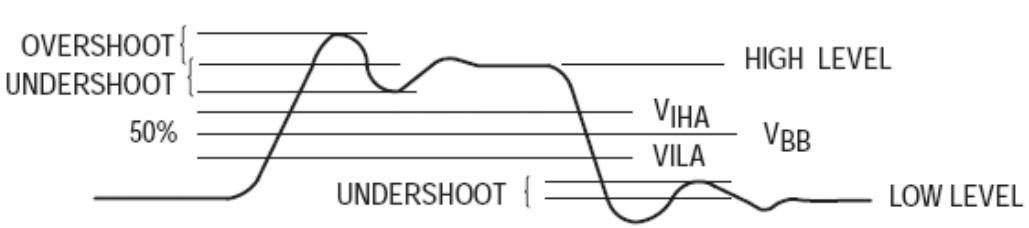
*$V_{OHA\ min} = V_{OH\ min}$, $V_{OLA\ max} = V_{OL\ max}$, $V_{IHA\ min} = V_{IH\ min}$ and $V_{ILA\ max} = V_{IL\ max}$ for MECL 10H.

Noise Margin Computations

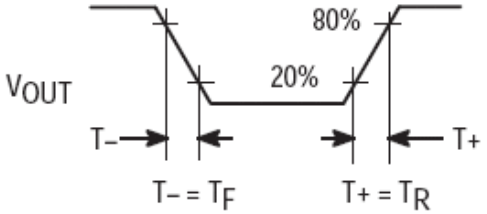
Family	Guaranteed Worst–Case dc Noise Margin (V)	Typical dc Noise Margin (V)
MECL 10H	0.150	0.270
MECL 10K	0.125	0.210

Familias Lógicas

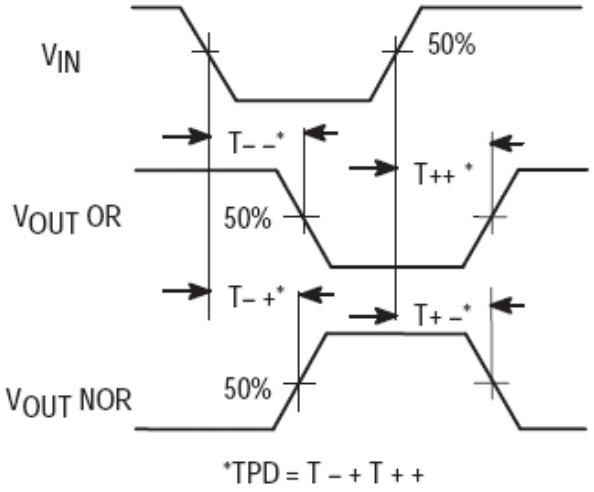
Formas de onda típicas encontradas en señales de alta velocidad



MECL WAVEFORM TERMINOLOGY



MECL 10K and MECL 10H Rise and Fall Times



MECL Propagation Delay

Familias Lógicas

FAMILIA ECL

Compuerta AND-NAND ECL modelos MC10EP/100EP

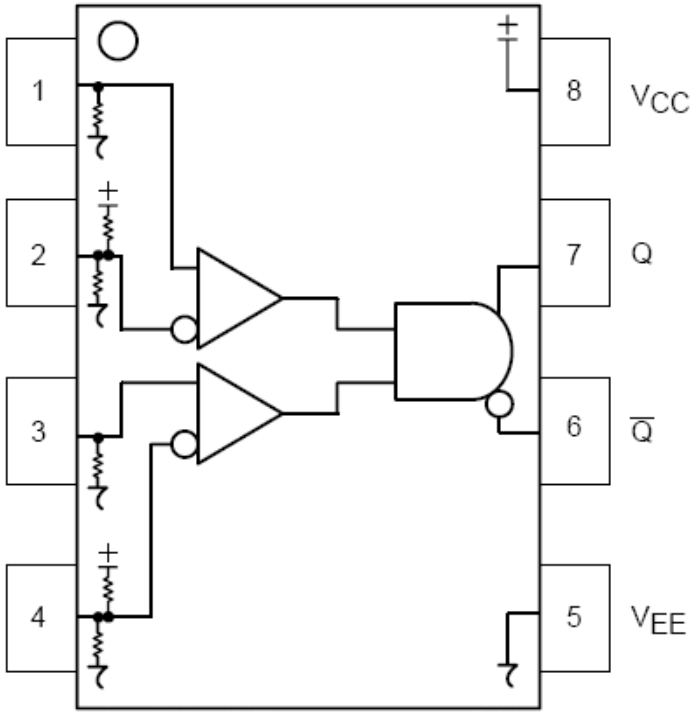
MC10EP05, MC100EP05

3.3V / 5V ECL 2-Input Differential AND/NAND

The MC10/100EP05 is a 2-input differential AND/NAND gate. The device is functionally equivalent to the EL05 and LVEL05 devices. With AC performance much faster than the LVEL05 device, the EP05 is ideal for applications requiring the fastest AC performance available.

The 100 Series contains temperature compensation.

- 220 ps Typical Propagation Delay
- Maximum Frequency > 3 GHz Typical
- PECL Mode Operating Range: V_{CC} = 3.0 V to 5.5 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = -3.0 V to -5.5 V
- Open Input Default State
- Safety Clamp on Inputs
- Q Output Will Default LOW with Inputs Open or at V_{EE}



Puede funcionar como PECL...!

Familias Lógicas

FAMILIA ECL

MC10EP05, MC100EP05

3.3V / 5V ECL 2-Input Differential AND/NAND

100EP DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 12)

Symbol	Characteristic	-40 °C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	15	25	32	17	27	36	19	28	38	mA
V_{OH}	Output HIGH Voltage (Note 13)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 13)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2075		2420	2075		2420	2075		2420	mV
V_{IL}	Input LOW Voltage (Single Ended)	1355		1675	1355		1675	1355		1675	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 14)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 -150			0.5 -150			0.5 -150			µA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

12. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.3 V to -2.2 V.
13. All loading with 50 ohms to V_{CC}-2.0 volts.
14. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

MC10EP05, MC100EP05

3.3V / 5V ECL 2-Input Differential AND/NAND

100EP DC CHARACTERISTICS, PECL V_{CC} = 5.0 V, V_{EE} = 0 V (Note 15)

Symbol	Characteristic	-40 °C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	15	25	32	17	27	36	19	28	38	mA
V_{OH}	Output HIGH Voltage (Note 16)	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV
V_{OL}	Output LOW Voltage (Note 16)	3055	3180	3305	3055	3180	3305	3055	3180	3305	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3775		4120	3775		4120	3775		4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3055		3375	3055		3375	3055		3375	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 17)	2.0		5.0	2.0		5.0	2.0		5.0	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 -150			0.5 -150			0.5 -150			µA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

15. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +2.0 V to -0.5 V.
16. All loading with 50 ohms to V_{CC}-2.0 volts.
17. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Familias Lógicas

FAMILIA ECL

MC10EP05, MC100EP05

3.3V / 5V ECL 2-Input Differential AND/NAND

100EP DC CHARACTERISTICS, NECL V_{CC} = 0 V, V_{EE} = -5.5 V to -3.0 V (Note 18)

Symbol	Characteristic	-40 °C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	15	25	32	17	27	36	19	28	38	mA
V_{OH}	Output HIGH Voltage (Note 19)	-1 145	-1020	-895	-1 145	-1020	-895	-1 145	-1020	-895	mV
V_{OL}	Output LOW Voltage (Note 19)	-1945	-1820	-1695	-1945	-1820	-1695	-1945	-1820	-1695	mV
V_{IH}	Input HIGH Voltage (Single Ended)	-1225		-880	-1225		-880	-1225		-880	mV
V_{IL}	Input LOW Voltage (Single Ended)	-1945		-1625	-1945		-1625	-1945		-1625	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 20)	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 -150			0.5 -150			0.5 -150			µA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

18. Input and output parameters vary 1:1 with V_{CC}.
19. All loading with 50 ohms to V_{CC}-2.0 volts.
20. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Familias Lógicas

FAMILIA ECL

MC10EP05, MC100EP05

3.3V / 5V ECL 2-Input Differential AND/NAND

AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = -3.0 V to -5.5 V or V_{CC} = 3.0 V to 5.5 V; V_{EE} = 0 V (Note 21)

Symbol	Characteristic	-40 °C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency (See Figure 2. F_{max}/JITTER)		> 3			> 3			> 3		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	160	210	260	170	220	270	210	260	320	ps
t_{JITTER}	Cycle-to-Cycle Jitter (See Figure 2. F_{max}/JITTER)		0.2	< 1		0.2	< 1		0.2	< 1	ps
V_{PP}	Input Voltage Swing (Differential)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times Q (20% - 80%)	70	120	170	80	130	180	100	150	200	ps

21. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 ohms to V_{CC}-2.0 V.

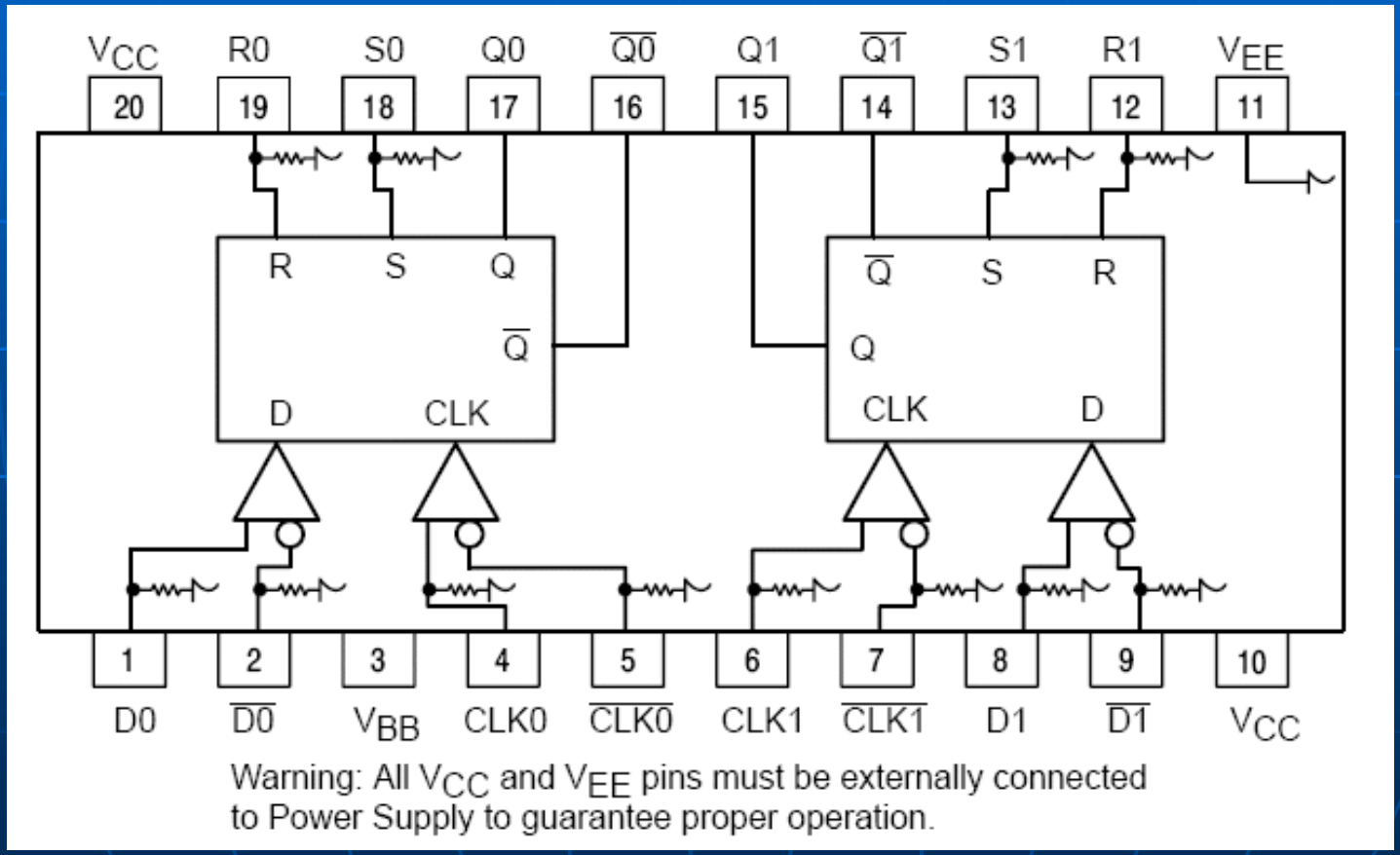
Familias Lógicas

Flip-Flop tipo D ECL modelos MC10EP/100EP

MC10EP29, MC100EP29

3.3V / 5V ECL Dual Differential Data and Clock D Flip-Flop With Set and Reset

FAMILIA ECL



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Familias Lógicas

Flip-Flop tipo D ECL modelos MC10EP/100EP

MC10EP29, MC100EP29

3.3V / 5V ECL Dual Differential Data and Clock D Flip-Flop With Set and Reset

FAMILIA ECL

AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = -3.0 V to -5.5 V or V_{CC} = 3.0 V to 5.5 V; V_{EE} = 0 V (Note 21)

Symbol	Characteristic		-40 °C			25°C			85°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency (See Figure 5 F_{max}/JITTER)			> 3.0			> 3.0			> 3.0		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	CLK	300	380	450	350	420	500	400	470	550	ps
		S	275	380	475	300	400	500	350	450	550	
		R	300	400	500	325	420	525	375	470	575	
t_S	Setup Time		100	20		100	20		100	20		ps
t_H	Hold Time		100	20		100	20		100	20		
t_{RR}/t_{RR2}	Set/Reset Recovery		150	80		150	80		150	80		ps
t_{PW}	Minimum Pulse Width	Set, Reset	500	300		500	300		500	300		ps
t_{JITTER}	Cycle-to-Cycle Jitter (See Figure 5 F_{max}/JITTER)			.2	< 1		.2	< 1		.2	< 1	ps
V_{PP}	Input Voltage Swing (Note 22)		150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times (20% - 80%)	Q, $\overline{Q}$	100	180	250	150	210	300	175	230	325	ps

21. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC}-2.0 V.
22. V_{PP}(min) is the minimum input swing for which AC parameters are guaranteed.

Familias Lógicas

FAMILIA ECL

Contador binario sincrónico ECL MC10EP016/100EP016

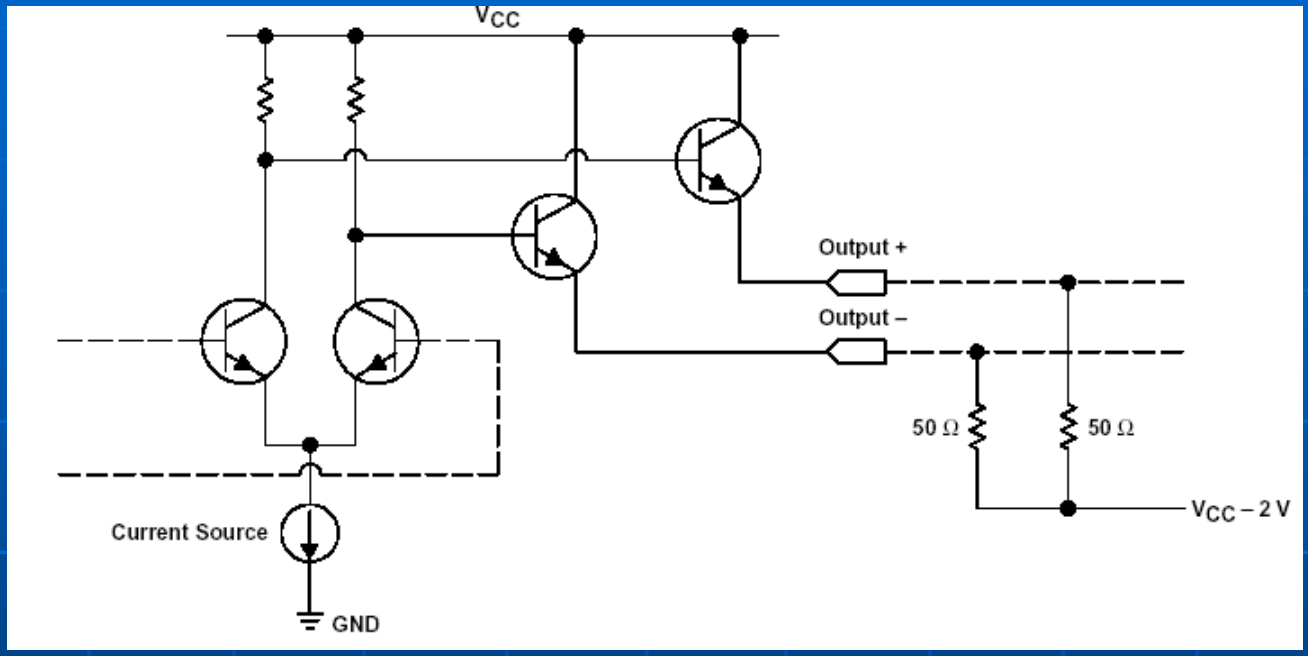
AC CHARACTERISTICS V_{EE} = -3.0 V to -5.5 V; V_{CC} = 0 V or V_{CC} = 3.0 V to 5.5 V; V_{EE} = 0 V (Note 25)

Symbol	Characteristic	-40 °C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{COUNT}	Maximum Frequency Q, $\overline{TC}$ COUT/$\overline{COUT}$		 > 1 > 800			 > 1 > 800			 > 1 > 800		 GHz MHz
t_{PLH} t_{PHL}	Propagation Delay (10) CLK to Q	300	460	600	350	500	650	400	560	700	ps
	(10) MR to Q	300	400	500	400	500	600	450	580	700	
	(10) CLK to $\overline{TC}$	350	420	550	400	500	600	400	550	700	
	(10) MR to $\overline{TC}$	250	350	450	350	450	550	400	510	600	
	(10) CLK to COUT	400	470	650	450	550	700	450	600	800	
	(10) MR to COUT	300	400	550	400	500	650	450	560	700	
	(100) CLK to Q	350	500	650	400	550	700	480	630	780	
	(100) MR to Q	400	550	700	450	590	750	520	670	820	
	(100) CLK to $\overline{TC}$	350	500	650	400	550	700	480	630	780	
	(100) MR to $\overline{TC}$	400	550	700	450	590	750	520	670	820	
	(100) CLK to COUT	400	550	750	450	600	800	530	680	880	
	(100) MR to COUT	450	600	800	500	640	850	570	720	920	
t_S	Setup Time Pn	100	-50		100	-50		100	-50		ps
	$\overline{CE}$	500	300		500	300		500	300		
	$\overline{PE}$	500	300		500	300		500	300		
	TCLD	500	300		500	300		500	300		
t_H	Hold Time Pn	100	-50		100	-50		100	-50		ps
	$\overline{CE}$	500	300		500	300		500	300		
	$\overline{PE}$	500	300		500	300		500	300		
	TCLD	500	300		500	300		500	300		
t_{JITTER}	Clock Random Jitter (RMS >1000 Waveforms)		2.6	8.5		2.5	8.0		2.5	8.0	ps
t_{RR}	Reset Recovery Time	200	80		200	80		200	80		ps
t_{PW}	Minimum Pulse Width CLK, MR	550	300		550	300		550	300		ps
t_r t_f	Output Rise/Fall Times 20% - 80%	120	210	320	120	220	320	150	250	450	ps

25. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC}-2.0 V.

Tecnología ECL

Etapa de salida LVPECL

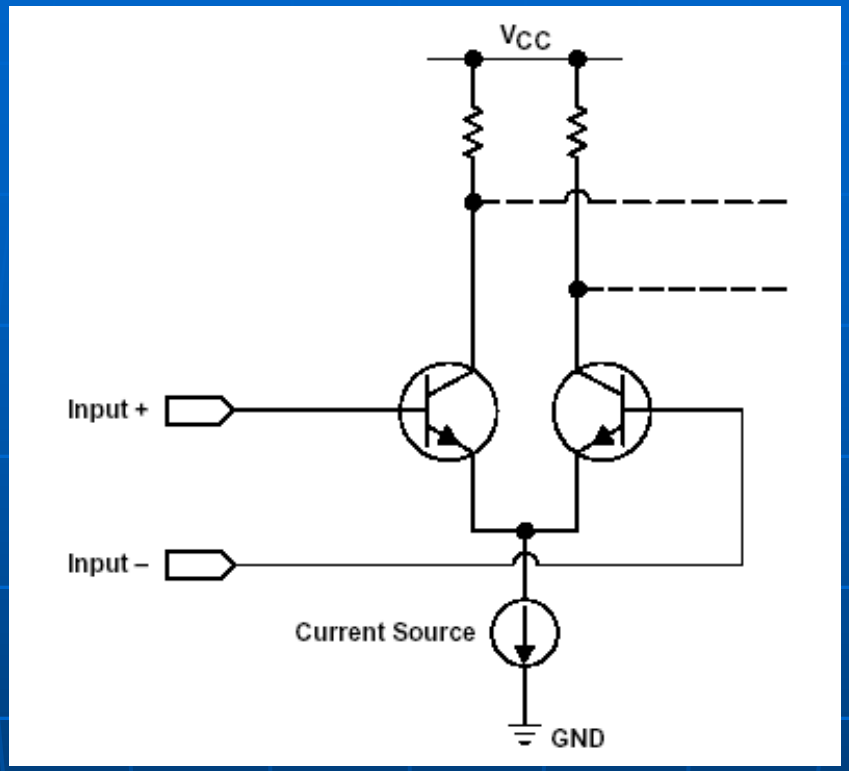


Salida diferencial seguidor por emisor trabajando en zona activa.
Permite tiempos de switching muy bajos a costa de un consumo permanente de corriente típico de 14 mA por las resistencias de Terminación de 50 ohms.
Impedancia de los seguidores es muy baja (4-5 ohms) por lo que hay que tener cuidado cuando se trabaj con líneas de transmisión por Posibles desadaptaciones.

Familias Lógicas

Tecnología ECL

Etapa de entrada LVPECL



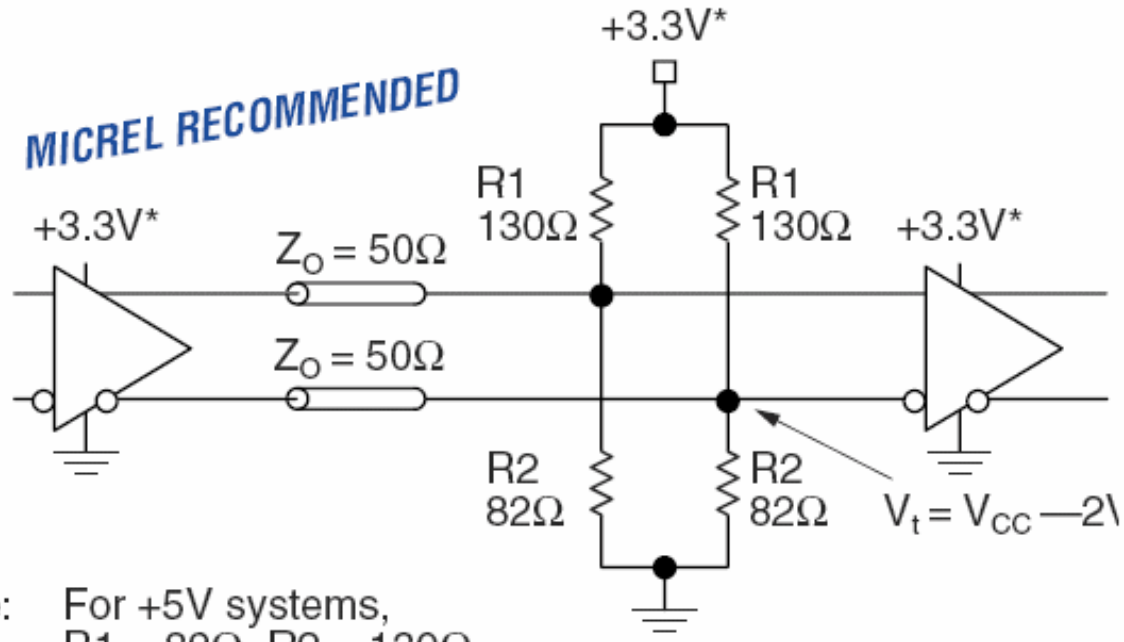
Entrada diferencial de alta impedancia.
Se requiere levantar la tensión de las entradas con resistencias de pull-up a una tensión de Vcc - 1,3 V a fin de proveer una tensión de modo común de 2,0 V (para el caso en que Vcc sea de +3,3V).

Tecnología ECL

Especificaciones LVPECL de Tensiones de entrada y salida

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	T_A = 0°C to +85°C	V_{CC} – 1.025		V_{CC} – 0.88	V
	T_A = –40°C	V_{CC} – 1.085		V_{CC} – 0.88	V
Output Low Voltage	T_A = 0°C to +85°C	V_{CC} – 1.81		V_{CC} – 1.62	V
	T_A = –40°C	V_{CC} – 1.83		V_{CC} – 1.55	V
Input High Voltage		V_{CC} – 1.16		V_{CC} – 0.88	V
Input Low Voltage		V_{CC} – 1.81		V_{CC} – 1.48	V

Terminación en dispositivos PECL-LVPECL

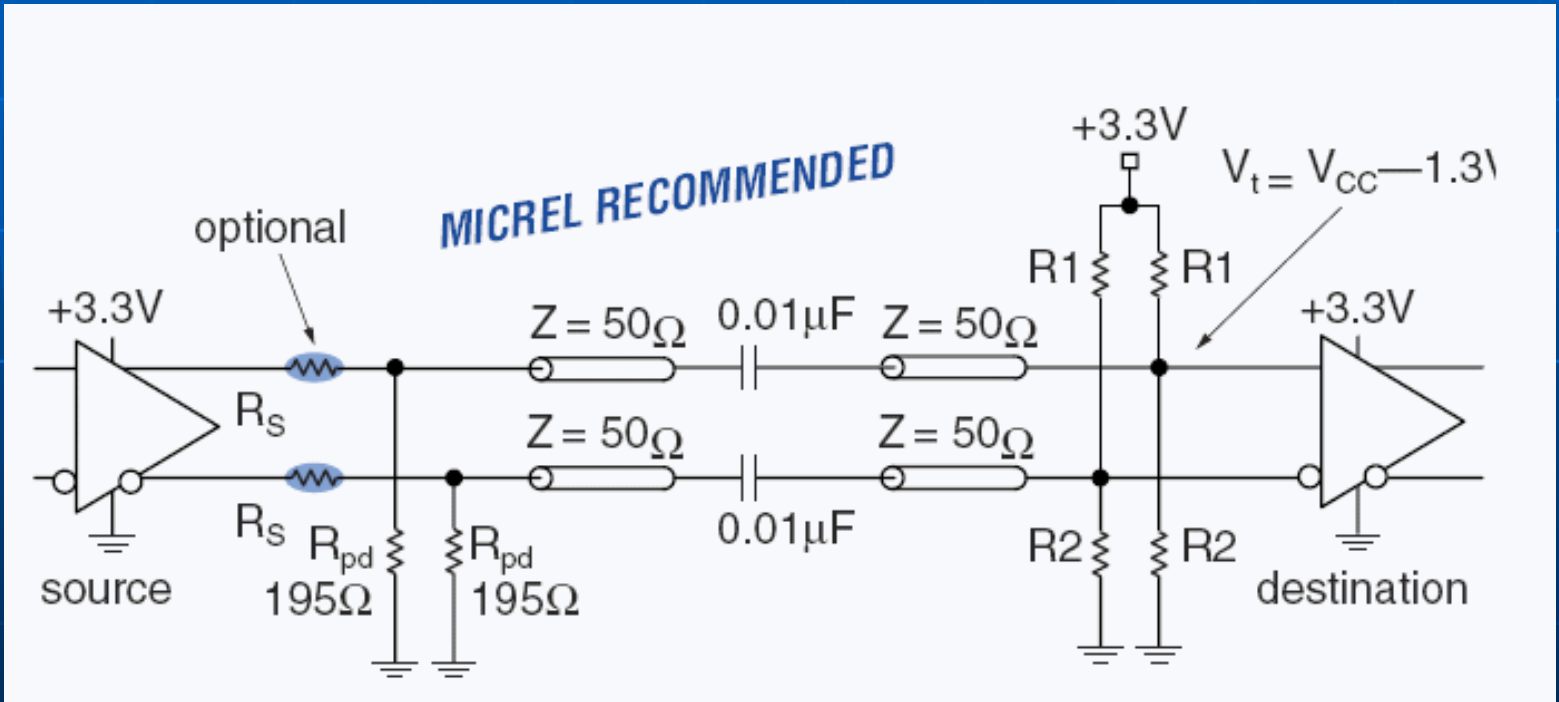


*Note: For +5V systems,
R1 = 82Ω, R2 = 130Ω

For +2.5V systems,
R1 = 250Ω, R2 = 62.5Ω

Familias Lógicas

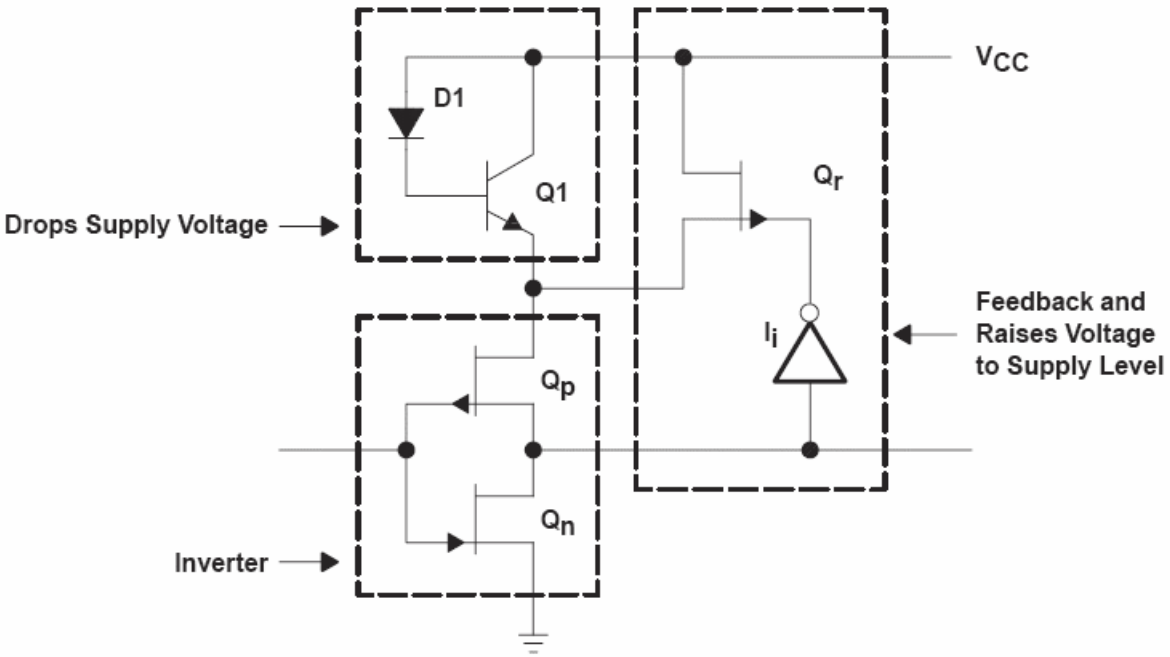
Desacople de DC en dispositivos PECL-LVPECL



Familias Lógicas

Tecnología BiCMOS (Bipolar - CMOS)

Familia ABT

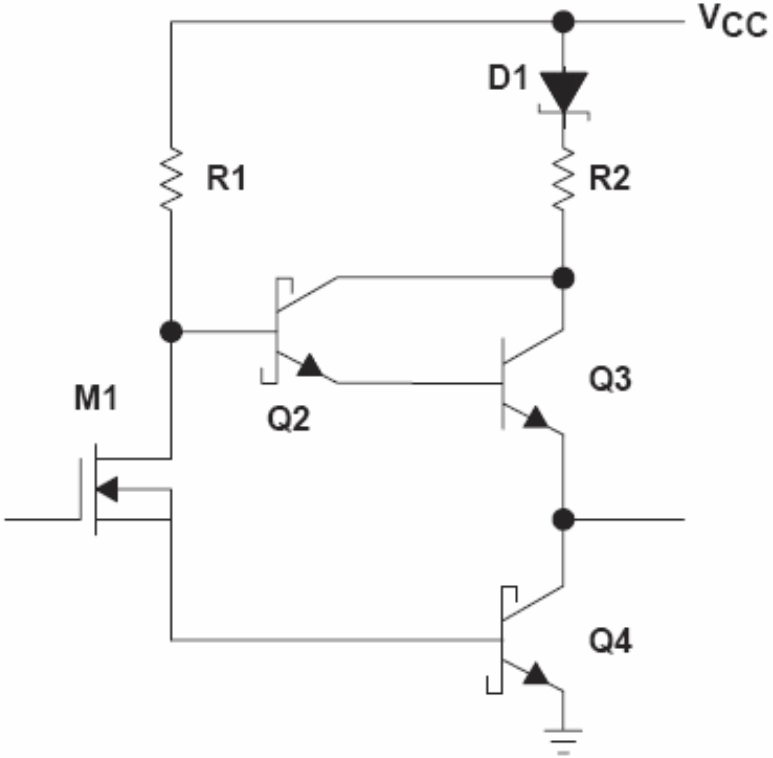


Entrada CMOS para bajo consumo.
D1 y Q1 sirven para disminuir la tensión de conmutación entre estados.
El circuito tiene una realimentación para generar histéresis y así aumentar el márgen de ruido.

Familias Lógicas

Tecnología BiCMOS

Familia ABT



Salida bipolar para disminuir el swing de tensión entre V_{OH} y V_{OL}. Mayor capacidad de corriente de carga.

Familias Lógicas

FAMILIA BICMOS

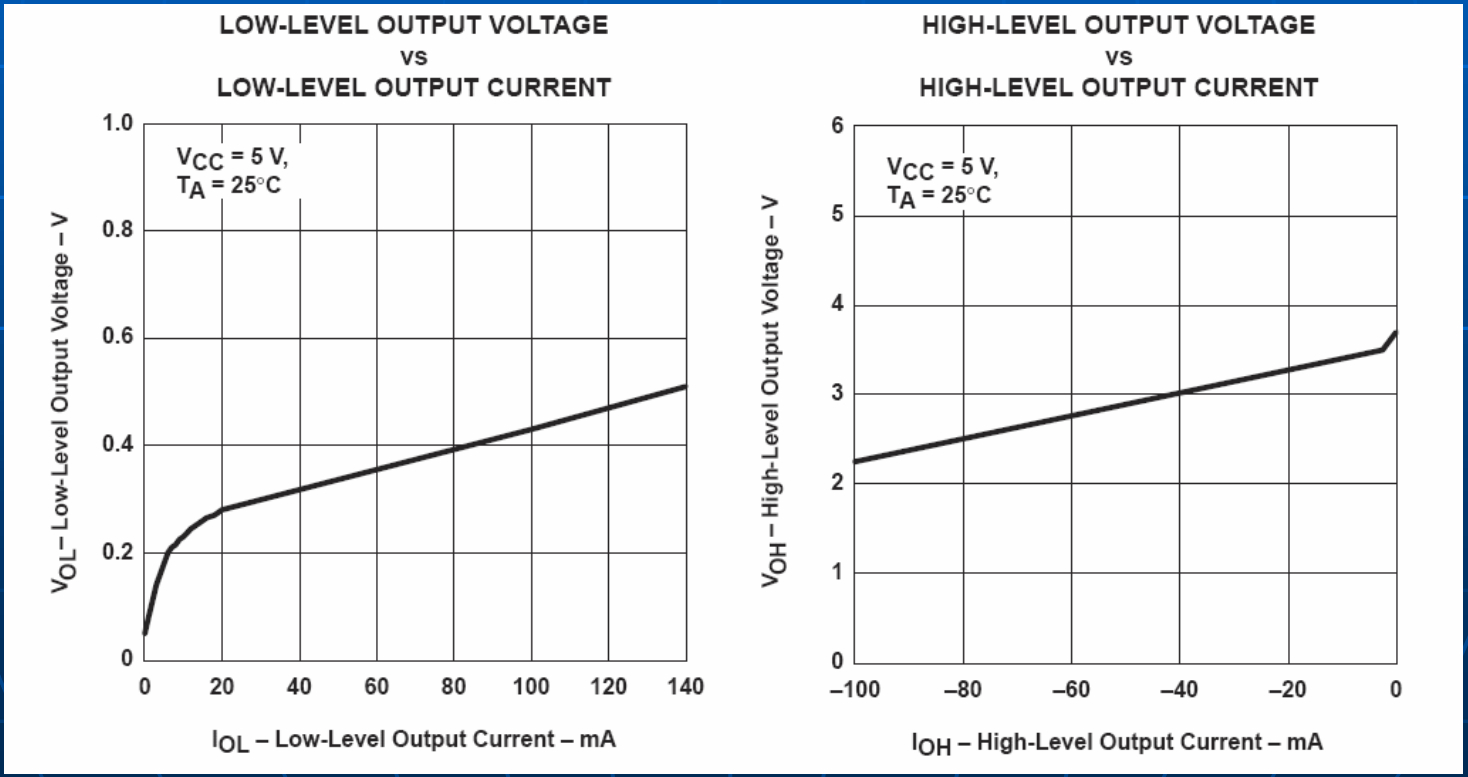
Tecnología BiCMOS

Familia ABT

Table 2. Input Current Specifications

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT245		SN74ABT245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND			±1		±1		±1	µA
I_{OZH}†	V_{CC} = 5.5 V,	V_O = 2.7 V			50		50		50	µA
I_{OZL}†	V_{CC} = 5.5 V,	V_O = 0.5 V			–50		–50		–50	µA

† The parameters I_{OZH} and I_{OZL} include the input leakage current.



Familias Lógicas

Tecnología BiCMOS

Familia ABT

Función de transferencia

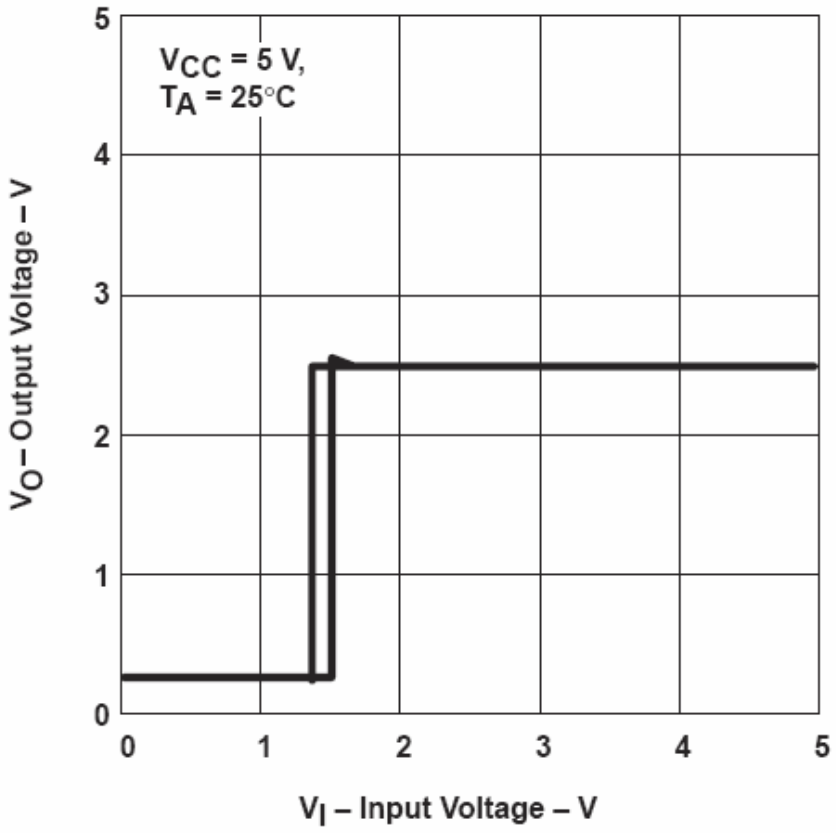


Gráfico de comparación entre Familias lógicas Icc vs. Frec.

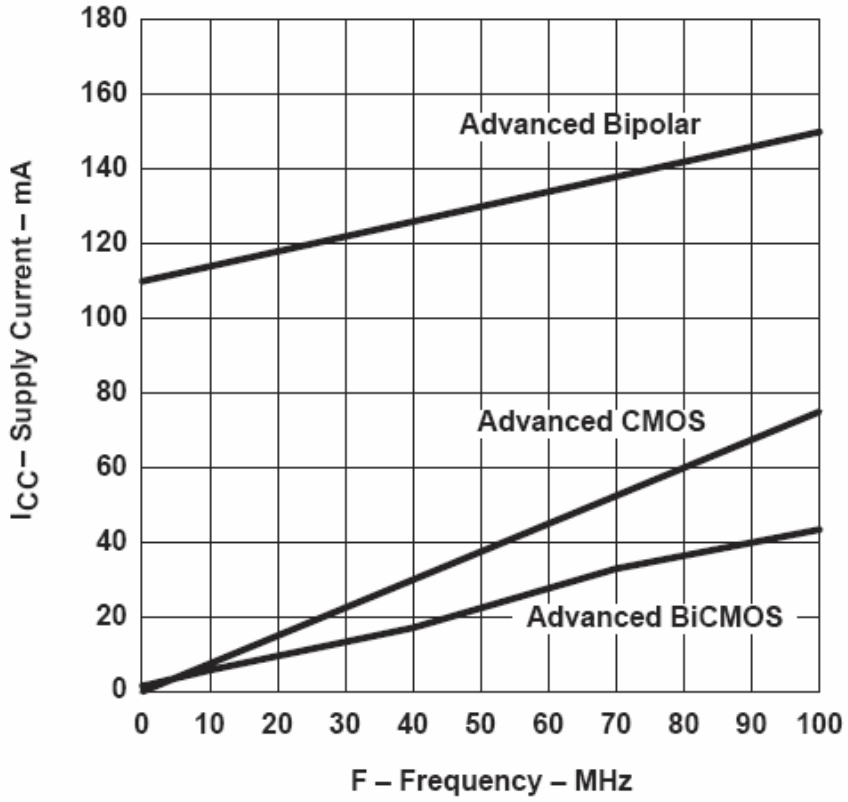
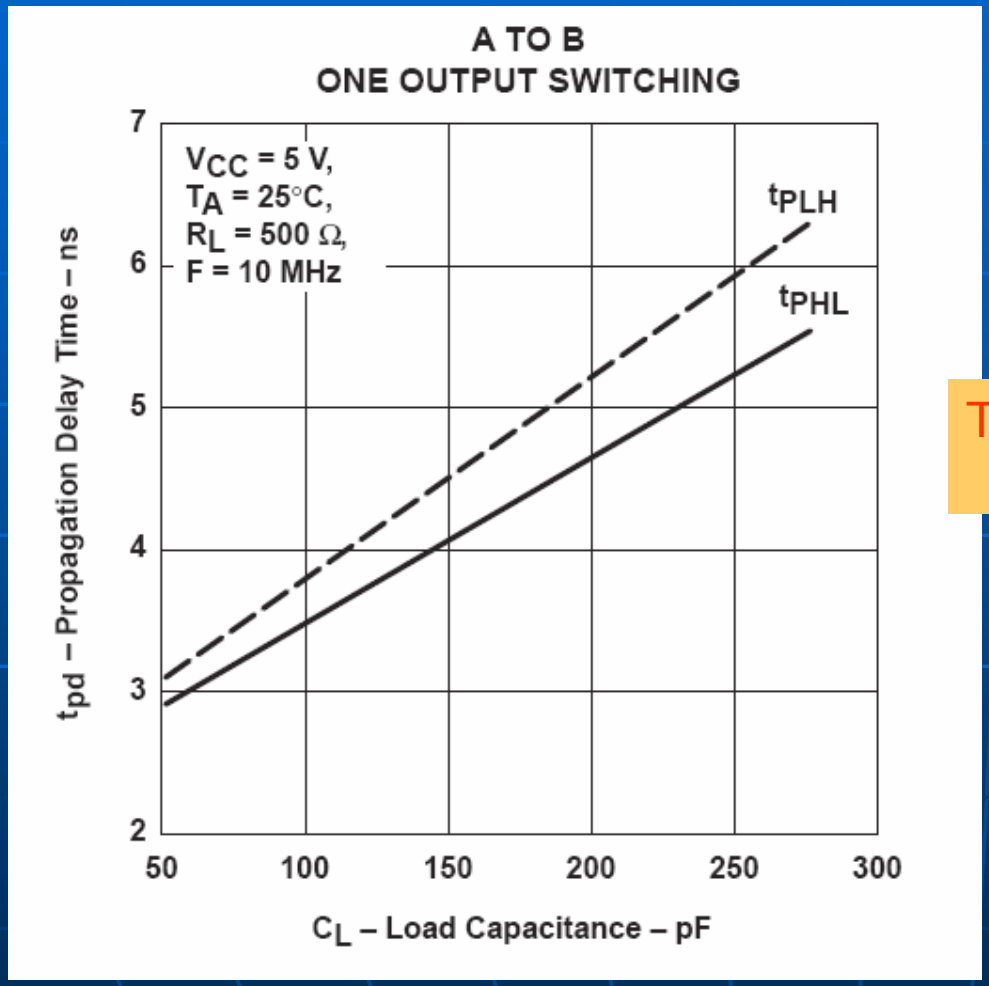


Figure 4. Supply Current vs Frequency

Familias Lógicas

Tecnología BiCMOS

Familia ABT

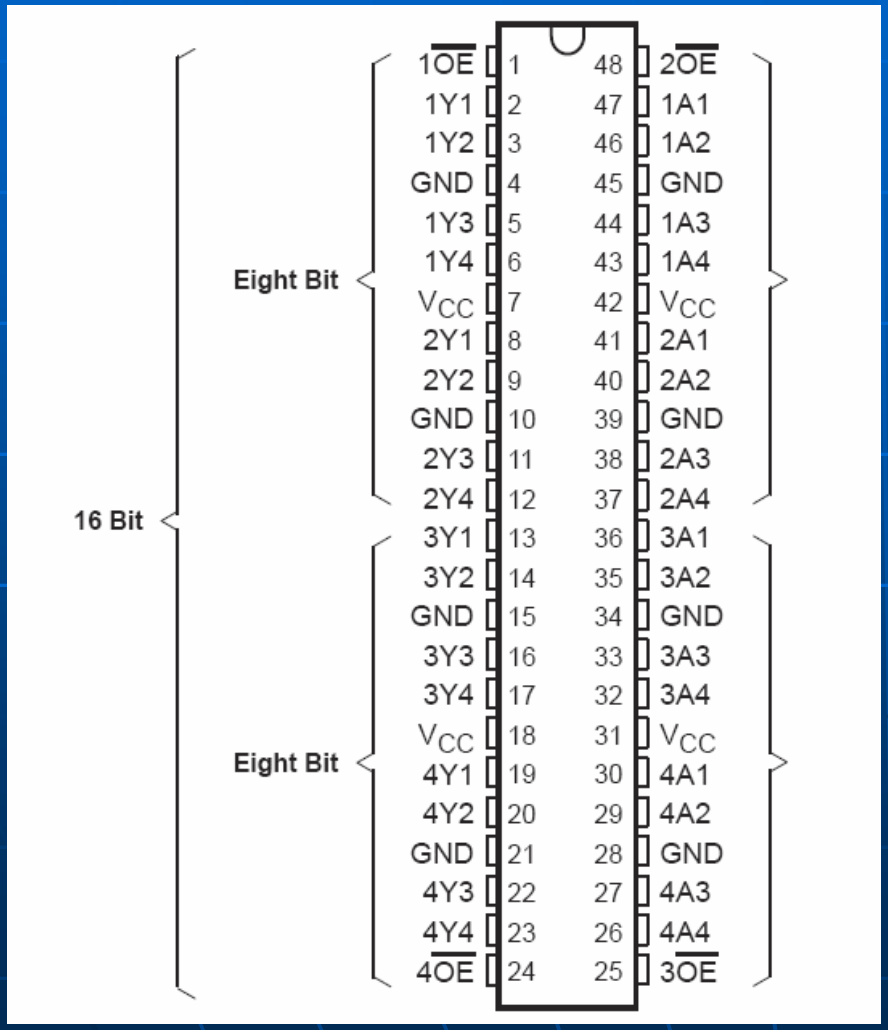


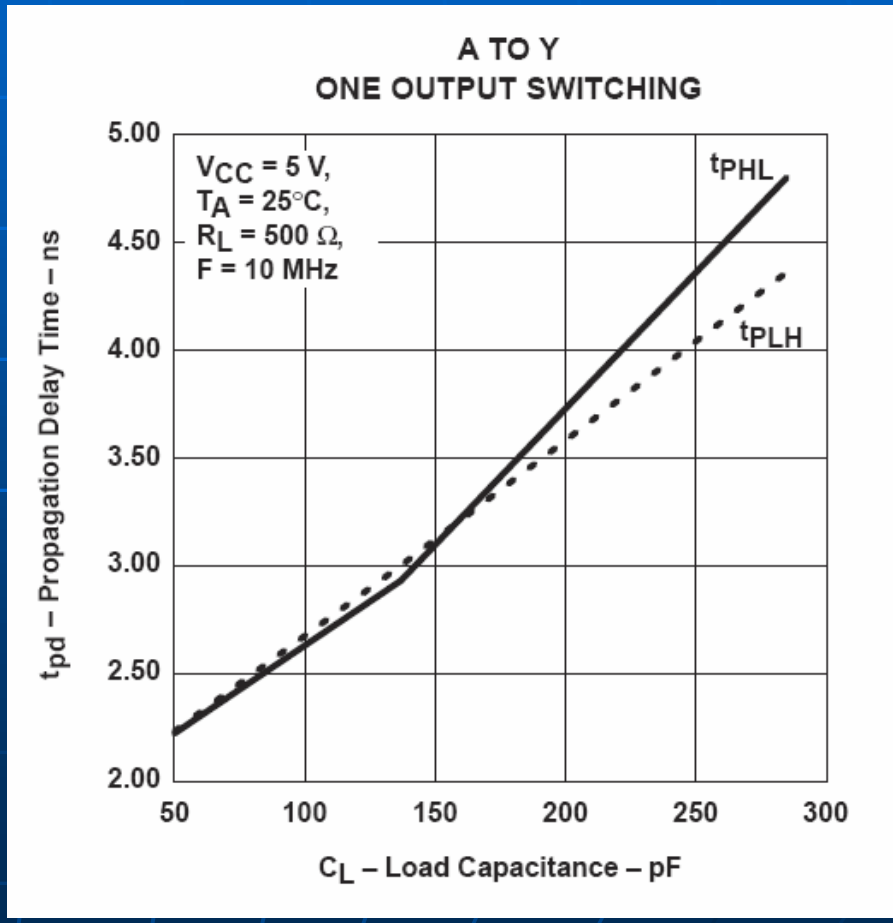
Tiempos de retardo promedio del órden de algunos [ns]

Familias Lógicas

Tecnología BiCMOS

Ejemplo 74ABT16244A: 16 buffer no inversor con tri-state





Familias Lógicas

Comparación de tecnologías en 5 V

5-V Logic

Technology	V_{CC} (V)	V_{CC} Range	t_{pd} max (ns)	I/O Tolerance (V)	Input Compatibility	Output Compatibility	Port	I_{OH} (max) (mA)	I_{OL} (max) (mA)	Static Current I_{CC} (µA)	Isolation Level*
Bipolar											
ALS	5	4.5 to 5.5	10.0	5	TTL	TTL	Both	Ð15	24	58 mA	0
AS	5	4.5 to 5.5	7.5	5	TTL	TTL	Both	Ð15	64	143 mA	0
74F	5	4.5 to 5.5	6.0	5	TTL	TTL	A	Ð3	24	120 mA	0
							B	Ð15	64		
LS	5	4.75 to 5.25	12.0	5	TTL	TTL	Both	Ð15	24	95 mA	0
S	5	4.75 to 5.25	9.0	5	TTL	TTL	Both	Ð15	64	180 mA	0
TTL	5	4.75 to 5.25	22.0	5	TTL	TTL	Both	Ð0.4	16	22 mA	0
BiCMOS											
ABT	5	4.5 to 5	3.5	5	LVTTL/TTL	TTL	Both	Ð32	64	250	1
ABTE	5	4.5 to 5.5	5.2	5	ETL	TTL	A	Ð60	90	48	1
							B	Ð12	12		
BCT	5	4.5 to 5.5	6.6	5	LVTTL/TTL	TTL	A	Ð3	24	90 mA	2
							B	Ð15	64		
CMOS											
AC	5	3.0 to 5.5	6.5	V_{CC} + 0.5	CMOS	CMOS	Both	Ð24	24	40	0
ACT	5	4.5 to 5.5	8.0	V_{CC}	TTL	CMOS	Both	Ð24	24	40	0
AHC	5	2.0 to 5.5	7.5	5.5**	CMOS	CMOS	Both	Ð8	8	40	0
AHC1G	5	2.0 to 5.5	5.0	5.5**	CMOS	CMOS	Both	Ð8	8	10	0
AHCT	5	4.5 to 5.5	7.7	5.5**	TTL	CMOS	Both	Ð8	8	40	0
AHCT1G	5	4.5 to 5.5	5.0	5.5**	TTL	CMOS	Both	Ð8	8	40	0
CBT	5	4.0 to 5.5	0.25	5.5	TTL	TTL	Both	N/A	N/A	3	0
CBT-C	5	4.0 to 5.5	0.25	5.5	TTL	TTL	Both	N/A	N/A	3	1
CBT1G	5	4.0 to 5.5	0.25	5.5	TTL	TTL	Both	N/A	N/A	1	0
CD4K	5,10,15	3.0 to 18.0	Ð	V_{CC}	CMOS	CMOS	Both	Ð0.2, Ð0.5, Ð1.4	0.52, 1.3, 3.6	5, 10, 20	0
FB (Q2040)	5	Ð	8.2	5	LVTTL/TTL	BTL	A	Ð3	24	70 mA	3
		Ð			BTL	LVTTL/TTL	B	N/A	100		
FCT	5	4.75 to 5.25	5.3	5	TTL	TTL	Both	Ð15	64	80	0
HC	5	2.0 to 6.0	21.0	V_{CC}	CMOS	CMOS	Both	Ð7.8	7.8	80	0
HCT	5	4.5 to 5.5	30.0	V_{CC}	TTL	CMOS	Both	Ð6	6	80	0

Familias Lógicas

Comparaciones entre familias LS-TTL y CMOS de alta velocidad

FACT = 24/–24 mA
ALS = 24/–15 mA
LS = 8/–0.4 mA @ 4.75 V V_{CC}
HC = 4/–4 mA

Corriente máxima de salida

FACT = 2 to 6 V
ALS = 5 V ± 10%
LS = 5 V ± 5%
HC = 2 to 6 V

Rango de tensiones de alimentación

FACT = 1.25/1.25 V
ALS = 0.4/0.7 V
LS = 0.3/0.7 V @ 4.75 V V_{CC}
HC = 0.8/1.25 V

Márgenes de ruido

Familias Lógicas

Comparaciones entre familias LS-TTL y CMOS de alta velocidad

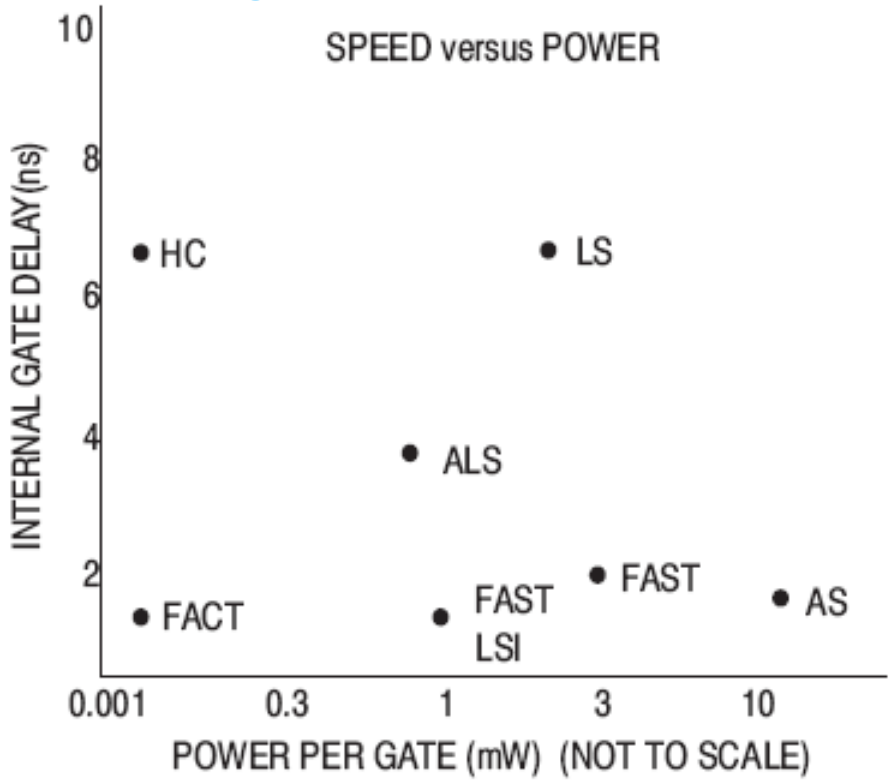
FACT	=	0.1 mW/Gate
ALS	=	1.2 mW/Gate
LS	=	2.0 mW/Gate
HC	=	0.1 mW/Gate

Consumo interno por compuerta

Ejemplo de retardos para un decodificador del tipo 74XX138

FACT	=	6.0 ns @ C_L	=	50 pF
ALS	=	12.0 ns @ C_L	=	50 pF
LS	=	22.0 ns @ C_L	=	15 pF
HC	=	17.5 ns @ C_L	=	50 pF

Curva general de velocidad vs potencia



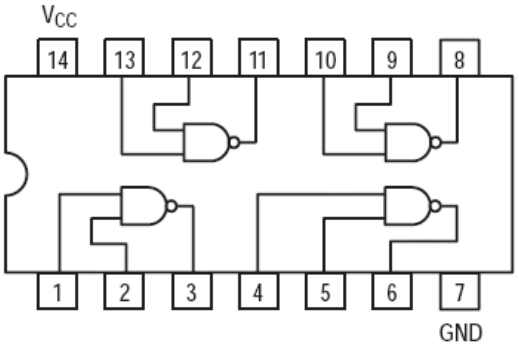
NOTA: En estas curvas la sigla FACT corresponde a una línea comercial de CMOS de alta velocidad como la ACT.

Familias Lógicas

SN74LS00

Quad 2-Input NAND Gate

- ESD > 3500 Volts



AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH}	Turn–Off Delay, Input to Output		9.0	15	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL}	Turn–On Delay, Input to Output		10	15	ns	

Familias Lógicas

MC74HC00A

Quad 2-Input NAND Gate

High–Performance Silicon–Gate CMOS

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0	75	95	110	ns
		3.0	30	40	55	
		4.5	15	19	22	
		6.0	13	16	19	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	16	19	
C_{in}	Maximum Input Capacitance		10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V, V_{EE} = 0 V	
C_{PD}	Power Dissipation Capacitance (Per Buffer)*	22	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

Familias Lógicas

MC74AC00, MC74ACT00

Quad 2-Input NAND Gate

High–Performance Silicon–Gate CMOS

AC CHARACTERISTICS ($t_r = t_f = 3.0$ nS; $C_L = 50$ pF; see Figures 3 and 4 for Waveforms)

Symbol	Parameter	V_{CC}* (V)	MC74AC00							Unit
			T_A = +25°C			T_A = –40°C to +85°C		T_A = –55°C to + 125°C		
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	3.3	2.0	7.0	9.5	2.0	10.0	1.0	11.0	ns
		5.0	1.5	6.0	8.0	1.5	8.5	1.0	8.5	
t_{PHL}	Propagation Delay	3.3	1.5	5.5	8.0	1.0	8.5	1.0	9.0	ns
		5.0	1.5	4.5	6.5	1.0	7.0	1.0	7.0	

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC CHARACTERISTICS ($t_r = t_f = 3.0$ nS; $C_L = 50$ pF; see Figures 3 and 4 for Waveforms)

Symbol	Parameter	V_{CC}* (V)	MC74ACT00							Unit
			T_A = +25°C			T_A = –40°C to +85°C		T_A = –55°C to +125°C		
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	5.0	1.5	5.5	9.0	1.0	9.5	1.0	9.5	ns
t_{PHL}	Propagation Delay	5.0	1.5	4.0	7.0	1.0	8.0	1.0	8.0	ns

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

Familias Lógicas

SN74LS74A

Dual D-Type Positive Edge-Triggered Flip-Flop

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
f_{MAX}	Maximum Clock Frequency	25	33		MHz	Figure 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Clock, Clear, Set to Output		13	25	ns	Figure 1	
			25	40	ns		

AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
$t_{W(H)}$	Clock	25			ns	Figure 1	V_{CC} = 5.0 V
$t_{W(L)}$	Clear, Set	25			ns	Figure 2	
t_s	Data Setup Time — HIGH	20			ns	Figure 1	
	LOW	20			ns		
t_h	Hold Time	5.0			ns	Figure 1	

MC74HC74A

Dual D Flip-Flop with Set and Reset

High–Performance Silicon–Gate CMOS

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 3.0 4.5 6.0	6.0 15 30 35	4.8 10 24 28	4.0 8.0 20 24	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$ (Figures 1 and 4)	2.0 3.0 4.5 6.0	100 75 20 17	125 90 25 21	150 120 30 26	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Set or Reset to Q or $\overline{Q}$ (Figures 2 and 4)	2.0 3.0 4.5 6.0	105 80 21 18	130 95 26 22	160 130 32 27	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

Familias Lógicas

MC74AC74, MC74ACT74

AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C C_L = 50 pF			74AC T_A = –40°C to +85°C C_L = 50 pF		Unit	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	100 140	125 160	– –	95 125	– –	MHz	3–3
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3 5.0	5.0 3.5	8.0 6.0	12.5 9.0	4.0 3.0	13.0 10.0	ns	3–6
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3 5.0	4.0 3.0	10.5 8.0	12.0 9.5	3.5 2.5	13.5 10.5	ns	3–6
t_{PLH}	Propagation Delay C_{Pn} to Q_n or $\overline{Q}_n$	3.3 5.0	4.5 3.5	8.0 6.0	13.5 10.0	4.0 3.0	16.0 10.5	ns	3–6
t_{PHL}	Propagation Delay C_{Pn} to Q_n or $\overline{Q}_n$	3.3 5.0	3.5 2.5	8.0 6.0	14.0 10.0	3.5 2.5	14.5 10.5	ns	3–6

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

Familias Lógicas

MC74AC74, MC74ACT74

AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C C_L = 50 pF			74ACT T_A = –40°C to +85°C C_L = 50 pF		Unit	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	145	210	–	125	–	MHz	3–3
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	3.0	5.5	9.5	2.5	10.5	ns	3–6
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	3.0	6.0	10.0	3.0	11.5	ns	3–6
t_{PLH}	Propagation Delay C_{Pn} to Q_n or $\overline{Q}_n$	5.0	4.0	7.5	11.0	4.0	13.0	ns	3–6
t_{PHL}	Propagation Delay C_{Pn} to Q_n or $\overline{Q}_n$	5.0	3.5	6.0	10.0	3.0	11.5	ns	3–6

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

Familias Lógicas

SN74LS161A SN74LS163A

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f_{MAX}	Maximum Clock Frequency	25	32		MHz	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay Clock to TC		20 18	35 35	ns	
t_{PLH} t_{PHL}	Propagation Delay Clock to Q		13 18	24 27	ns	
t_{PLH} t_{PHL}	Propagation Delay CET to TC		9.0 9.0	14 14	ns	
t_{PHL}	$\overline{MR}$ or $\overline{SR}$ to Q		20	28	ns	

AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_WCP	Clock Pulse Width Low	25			ns	V_{CC} = 5.0 V
t_W	$\overline{MR}$ or $\overline{SR}$ Pulse Width	20			ns	
t_s	Setup Time, other*	20			ns	
t_s	Setup Time $\overline{PE}$ or $\overline{SR}$	25			ns	
t_h	Hold Time, data	3			ns	
t_h	Hold Time, other	0			ns	
t_{rec}	Recovery Time $\overline{MR}$ to CP	15			ns	

*CEP, CET, or DATA

Familias Lógicas

MC74HC161A, MC74HC163A

Presettable Counters

High–Performance Silicon–Gate CMOS

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	Fig.	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle)*	1, 7	2.0	6	5	4	MHz
			3.0	15	12	10	
			4.5	30	24	20	
			6.0	35	28	24	
t_{PLH}	Maximum Propagation Delay, Clock to Q	1, 7	2.0	120	160	200	ns
			3.0	75	120	150	
			4.5	20	23	28	
			6.0	16	20	22	
t_{PHL}		1, 7	2.0	145	185	220	ns
			3.0	100	135	150	
			4.5	22	25	30	
			6.0	18	20	23	

MC74AC161, MC74ACT161, MC74AC163, MC74ACT163

Synchronous Presettable Binary Counter

AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V_{CC}* (V)	74AC163 T_A = +25°C C_L = 50 pF			74AC163 T_A = –40°C to +85°C C_L = 50 pF		Unit	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Count Frequency	3.3 5.0	70 110	95 140	– –	60 95	– –	MHz	3–3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0	2.0 1.5	7.5 5.5	12.5 9.0	1.5 1.0	13.5 9.5	ns	3–6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0	1.5 1.5	8.5 6.0	12.0 9.5	1.5 1.5	13.0 10.0	ns	3–6
t_{PLH}	Propagation Delay CP to TC	3.3 5.0	3.0 2.0	9.5 7.0	15.0 10.5	2.5 1.5	16.5 11.5	ns	3–6
t_{PHL}	Propagation Delay CP to TC	3.3 5.0	3.5 2.0	11.0 8.0	14.0 11.0	2.5 2.0	15.5 11.5	ns	3–6
t_{PLH}	Propagation Delay CET to TC	3.3 5.0	2.0 1.5	7.5 5.5	9.5 6.5	1.5 1.0	11.0 7.5	ns	3–6
t_{PHL}	Propagation Delay CET to TC	3.3 5.0	2.5 2.0	8.5 6.0	11.0 8.5	2.0 1.5	12.5 9.5	ns	3–6

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
*Voltage Range 5.0 V is 5.0 V ±0.5 V.

Familias Lógicas

MC74AC161, MC74ACT161, MC74AC163, MC74ACT163

Synchronous Presettable Binary Counter

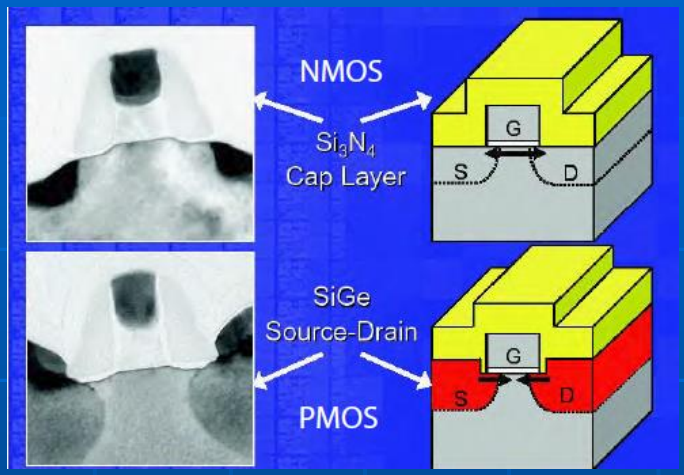
AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

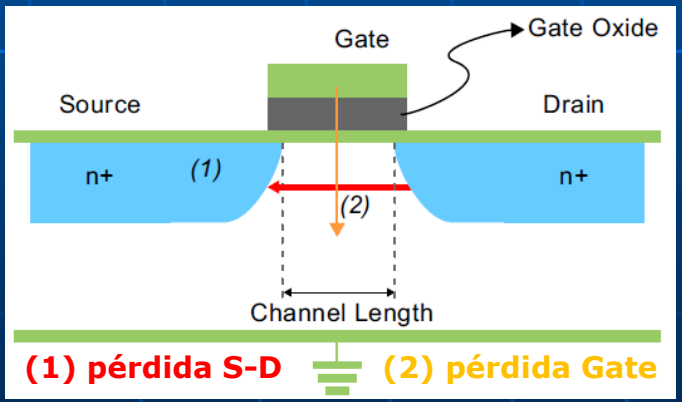
Symbol	Parameter	V_{CC}* (V)	74ACT163 T_A = +25°C C_L = 50 pF			74ACT163 T_A = –40°C to +85°C C_L = 50 pF		Unit	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Count Frequency	5.0	120	140	–	105	–	MHz	3–3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.5	5.5	10.0	1.5	11.0	ns	3–6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.5	6.0	11.0	1.5	12.0	ns	3–6
t_{PLH}	Propagation Delay CP to TC	5.0	2.5	7.0	11.5	2.0	13.5	ns	3–6
t_{PHL}	Propagation Delay CP to TC	5.0	3.0	8.0	13.5	2.0	15.0	ns	3–6
t_{PLH}	Propagation Delay CET to TC	5.0	2.0	5.5	9.0	1.5	10.5	ns	3–6
t_{PHL}	Propagation Delay CET to TC	5.0	2.0	6.0	10.0	2.0	11.0	ns	3–6

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

Avances en CMOS

A principios de la década del 2000, la necesidad de conseguir mayor velocidad de conmutación en CMOS, se solucionó empleando la técnica strained silicon la cual genera la compresión de átomos de Si en la red cristalina, mejorando la movilidad de los portadores. Intel emplea Si-Ge + Si en transistores PMOS y Si_3N_4 + Si en los del tipo NMOS.



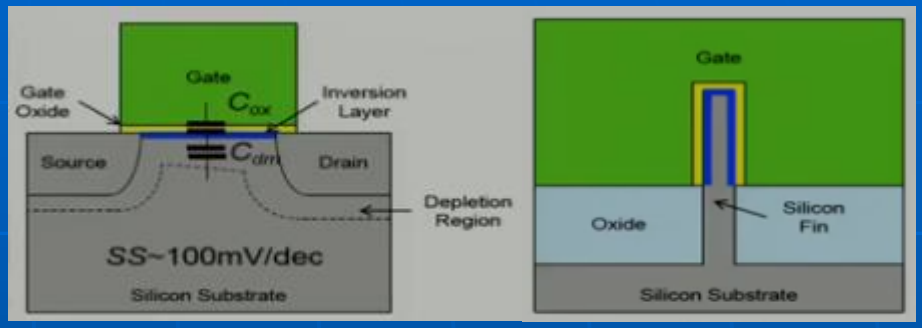


Por otro lado la estructura simple de un transistor CMOS no puede seguir utilizándose para valores de longitud de canal inferiores a 22 nm debido a ciertos efectos que empiezan a aparecer (short channel effects), como la pérdida de control del gate en la distribución de la corriente Ids, aumento de la corriente de pérdida para tensiones Vgate por debajo del umbral, etc.

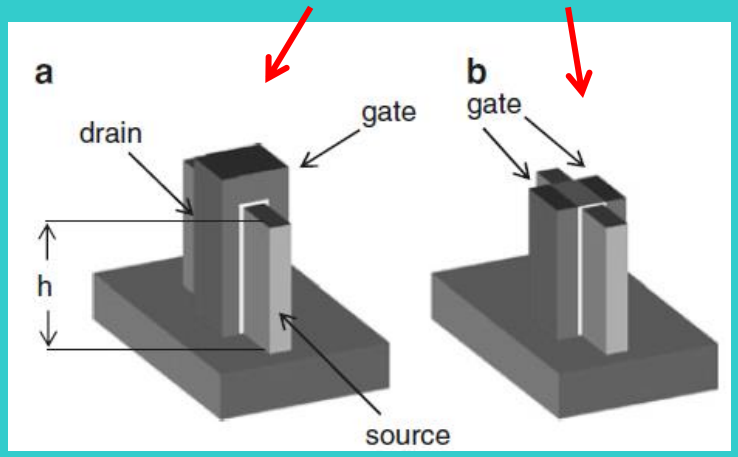
Debido a esto se han ideado varias estructuras mas complejas a fin de poder mejorar el rendimiento de un transistor (mejores velocidades de conmutación a menor disipación de potencia mientras se disminuye el tamaño físico).
Una de las actuales soluciones es el transistor es el FINFET multigate.

FET tipo Bulk

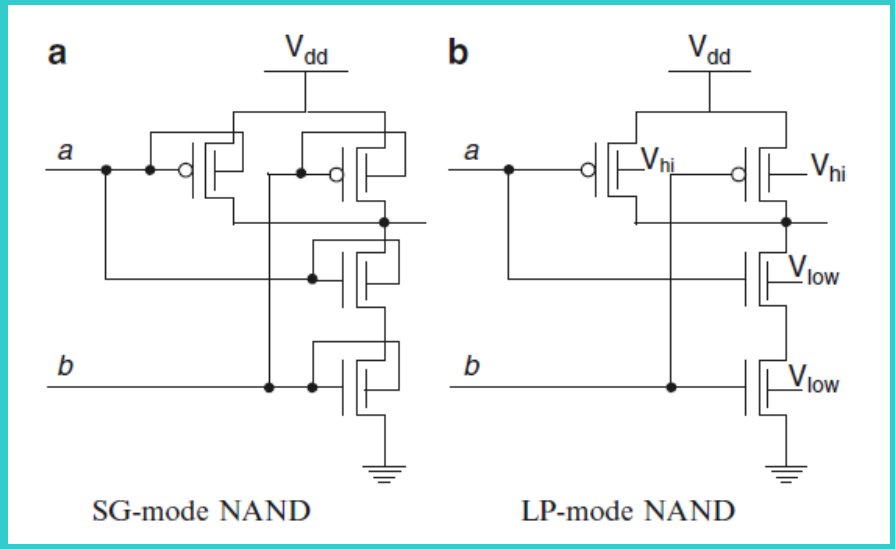
FINFET



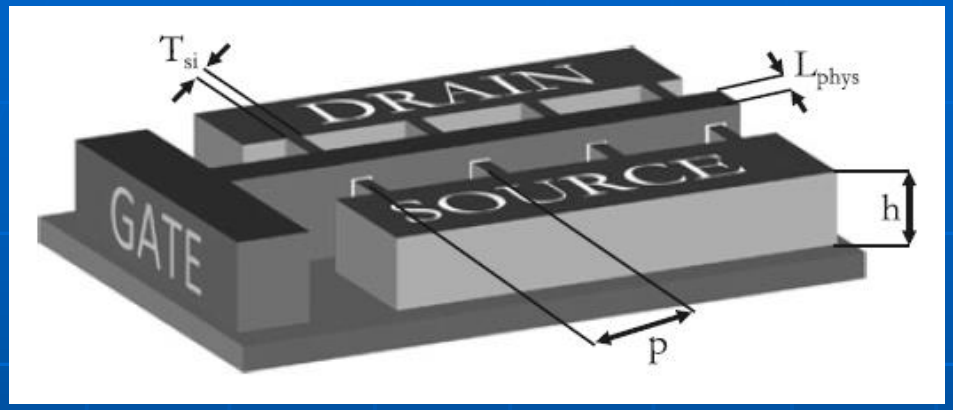
FINFET Short Gate/Isolate Gate



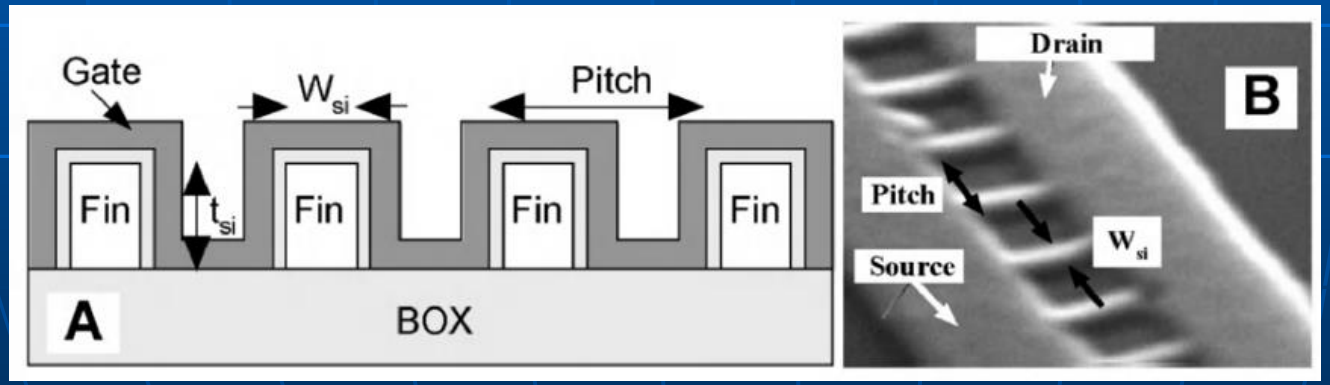
Ejemplo de aplicación en el diseño de una compuerta NAND



FINFET Multi Gate



Surge de la necesidad de aumentar la densidad de corriente de carga y de controlar mejor los efectos de "short channel".



Vista en corte

Foto con microscopio

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